CLASS 24

JFET PARAMETERS AND BIASING, D-MOSFET OPERATION AND BIASING, E-MOSFET OPERATION

2. r_d

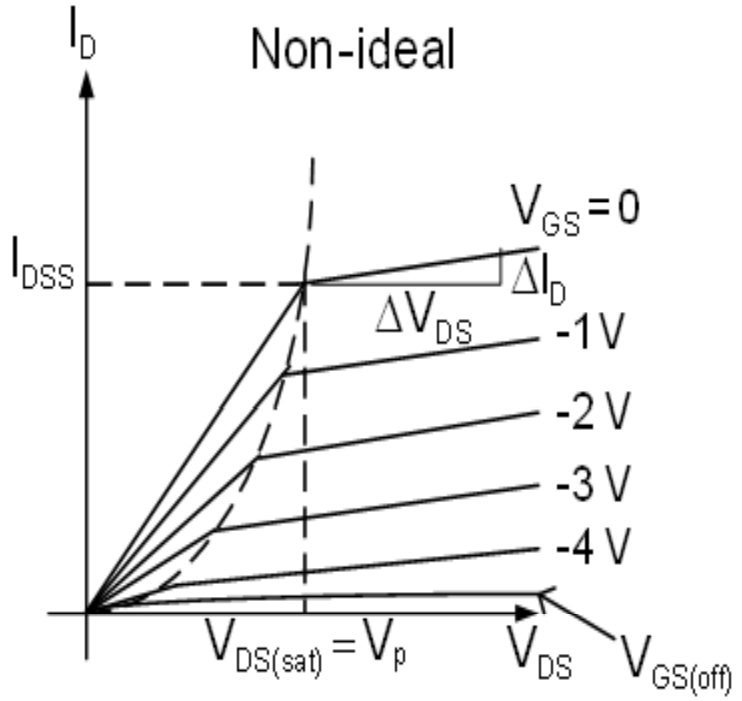
The next parameter of the JFET is the drain resistor, r_d. r_d is the ac resistance between D and S when the JFET is operating in the saturation region. r_d is the inverse of the slope of the drain characteristic in the saturation region. r_d is also the output resistance.

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\ \text{fixed}}$$

$$|Y_{os}| = \frac{1}{r_d}$$

$|Y_{os}|$ is the output admittance. Y_{os} is provided in the data sheet.

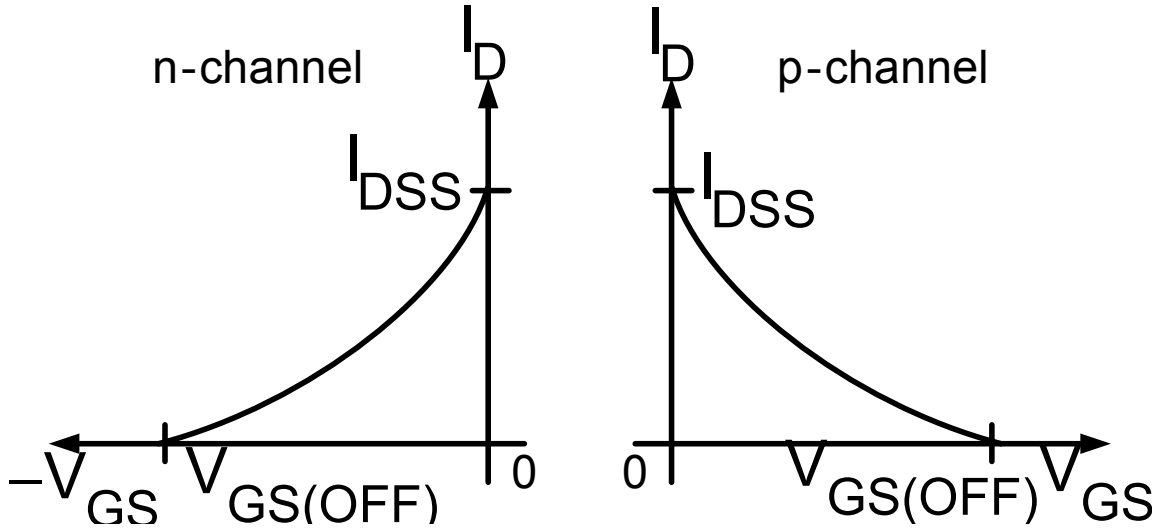
When r_d increases, Y_{os} decreases. Y_{os} is typically in the range of 10 to 50 μmho (or μS). Therefore, r_d is in the range of 20 to 100 kΩ.



- **The V_{GS} from 0 to $V_{GS(off)}$ controls the drain current that flows when the device is in its saturation/pinch-off region.**
- **When the JFET is biased in its saturation/pinched-off region, the equation that relates the drain current, I_D, with V_{GS} is represented by the following:**

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

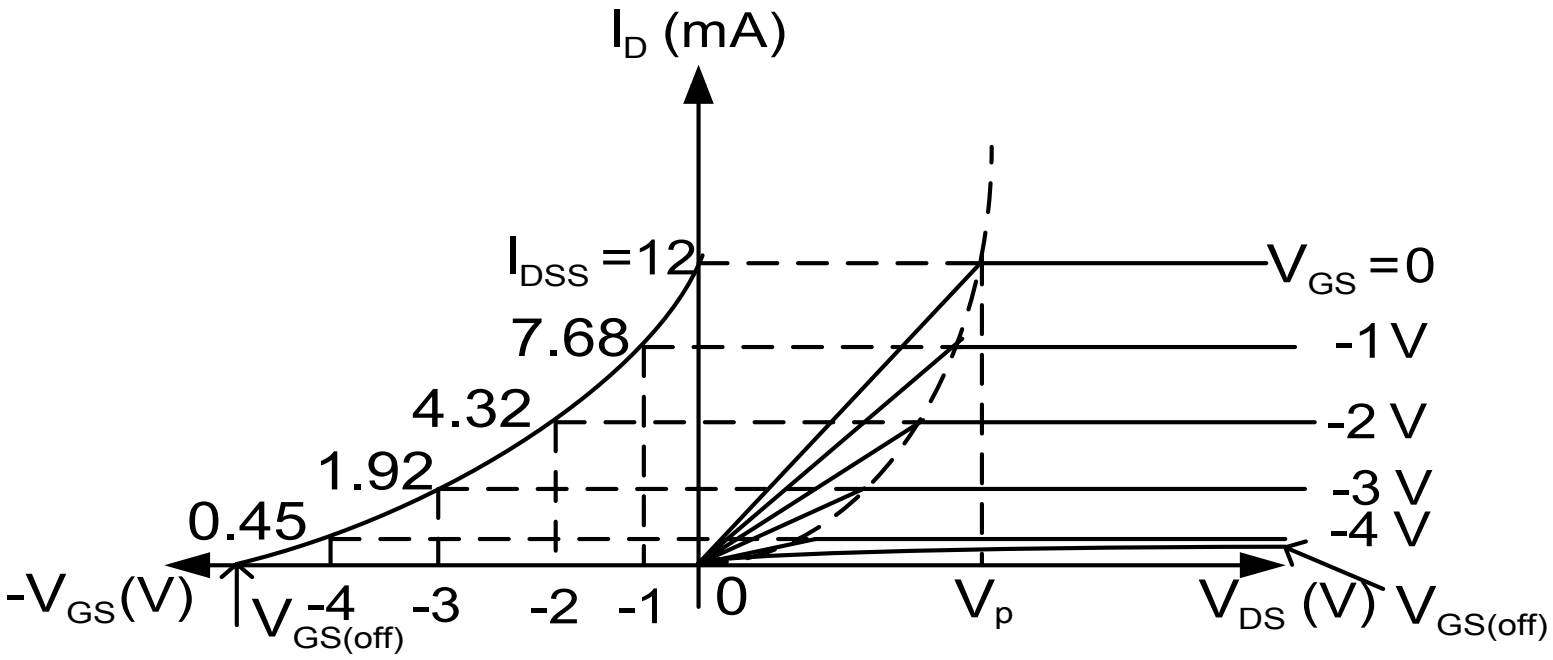
- **This equation contributes to why the JFET is known as square law device.**



- **The transfer function can be obtained/drawn from the drain characteristic as shown in the diagram below.**
- **The drain current can be calculated by using**

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

provided $V_{GS(off)}$ and I_{DSS} are known.



JFET BIASING

4 types of biasing circuit will be studied in this course:

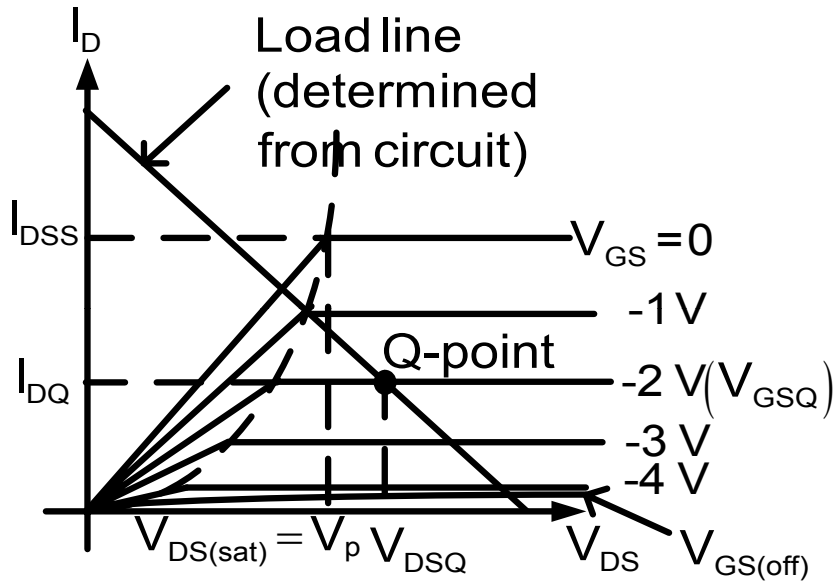
(i). Fixed biasing

(ii).Self biasing

(iii).Mid-point biasing

(iv).Voltage division biasing

Load line and Q-point for JFET



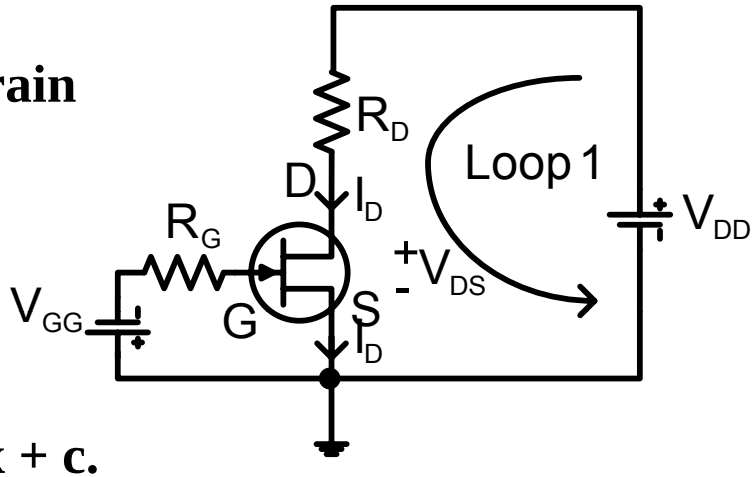
A load line connects 2 points on the drain characteristic. One point is on the I_D axis and the other is on the V_{DS} axis. For a known V_{GS}, the intercept point between the load line and the drain curve can determine the operating/quiescent (Q) point and consequently, the I_{DQ} and V_{DSQ}.

1. **Fixed biasing**

- **To determine the Q-point (I_{DQ} and V_{DSQ}), the relationship between the I_D and V_{DS} needs to be known.**
- **Looking at the output loop (Loop 1 - drain characteristic):**

$$-V_{DD} + I_D R_D + V_{DS} = 0$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$$

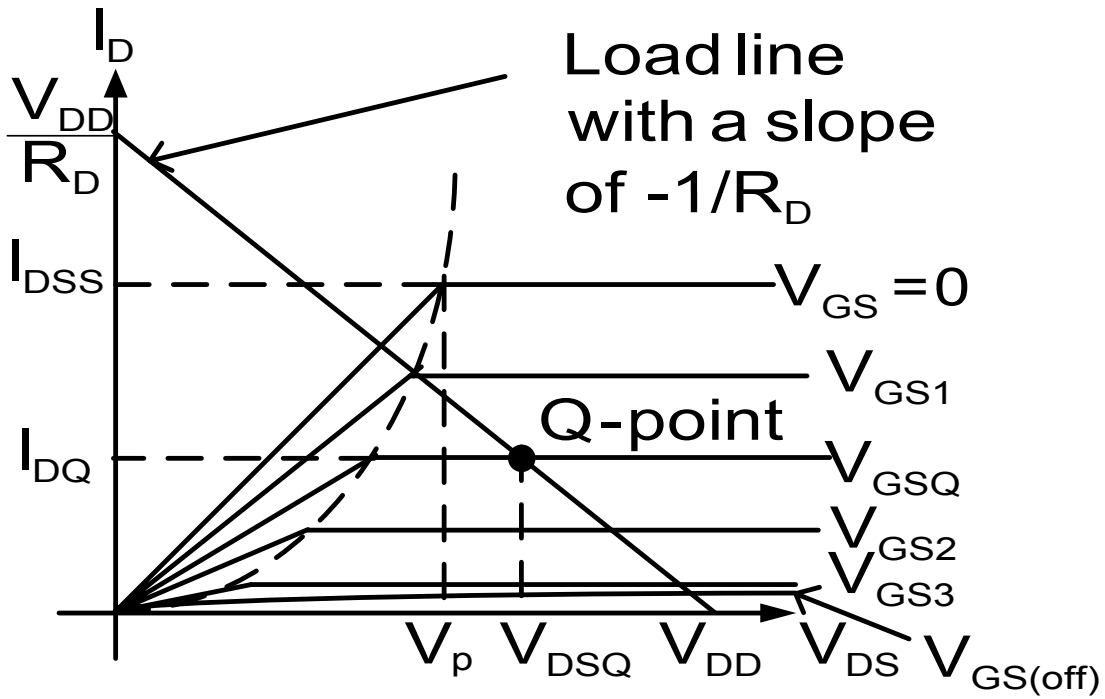


- **This expression is in the form of y = mx + c.**
- **Slope is $-\frac{1}{R_D}$ and c = $\frac{V_{DD}}{R_D}$.**

$$-V_{DD} + I_D R_D + V_{DS} = 0$$

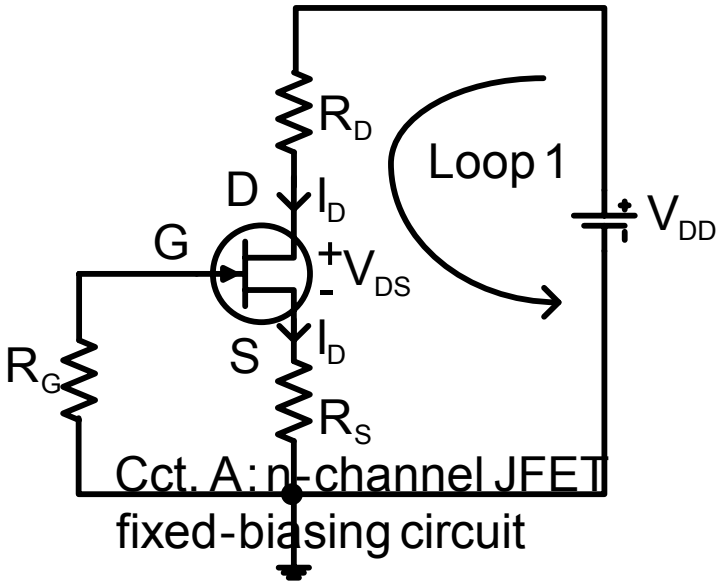
$$I_D = \frac{V_{DD} - V_{DS}}{R_D} = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$$

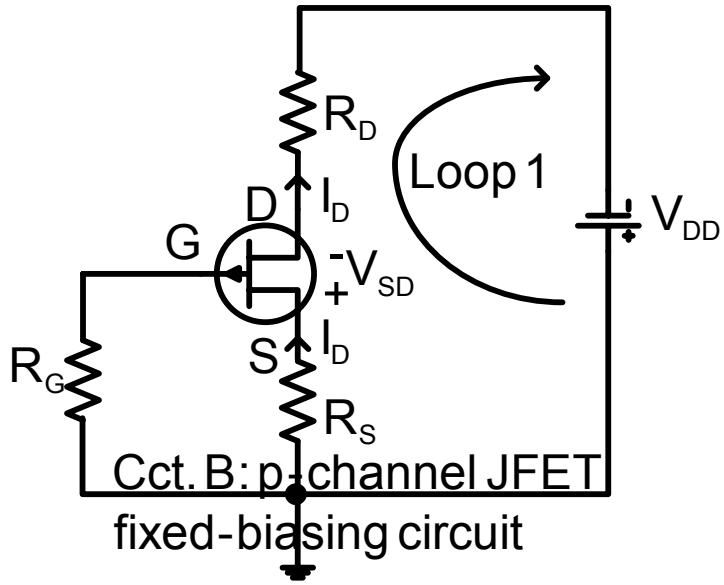
Slope is $-1/R_D$ and c = V_{DD}/R_D. At I_D=0, V_{DS}= V_{DD}. Hence, the load line intersects the I_D axis at V_{DD}/R_D and the V_{DS} axis at V_{DD}. Once V_{GSQ} is known, I_{DQ} and V_{DSQ} can be determined.



2. Self-biasing

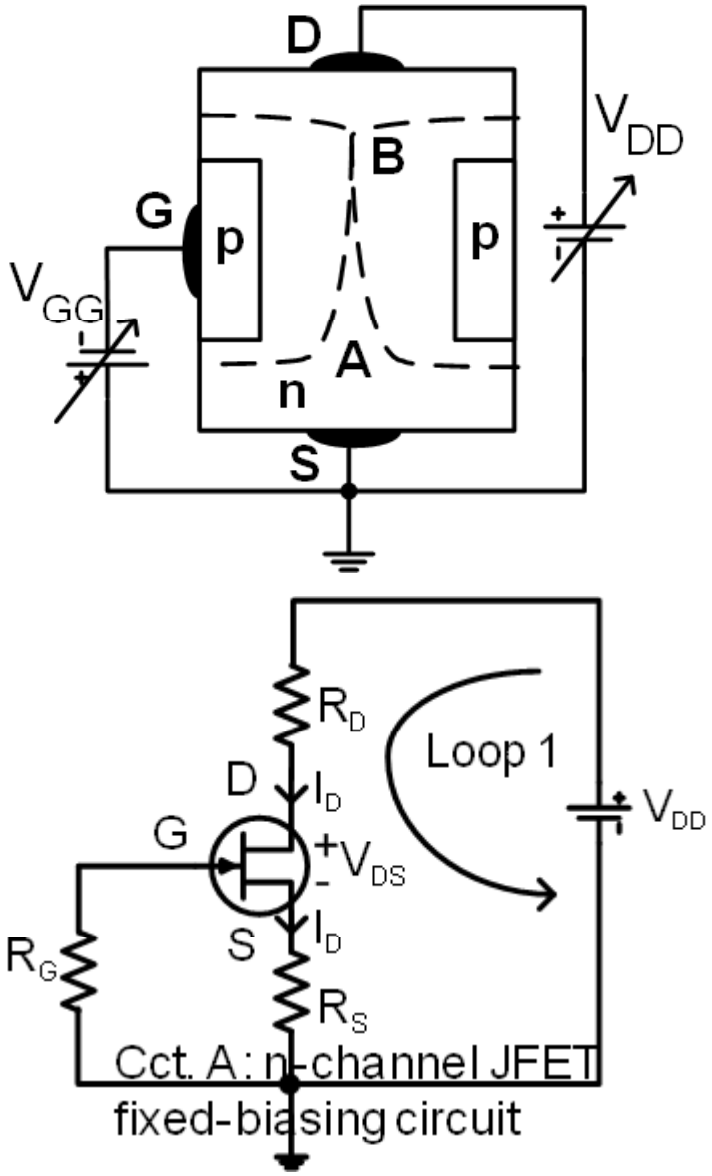
In order to operate in the saturation region (hence, as an amplifier), G-S of the JFET needs to be reverse biased. To obtain this condition, the V_{GS} has to be negative for the n-channel JFET and positive for the p-channel JFET. The following topologies will enable the mentioned condition to be achieved without the need of an external voltage to be connected to the G. Due to this capability, this topology is called self-biasing circuit.





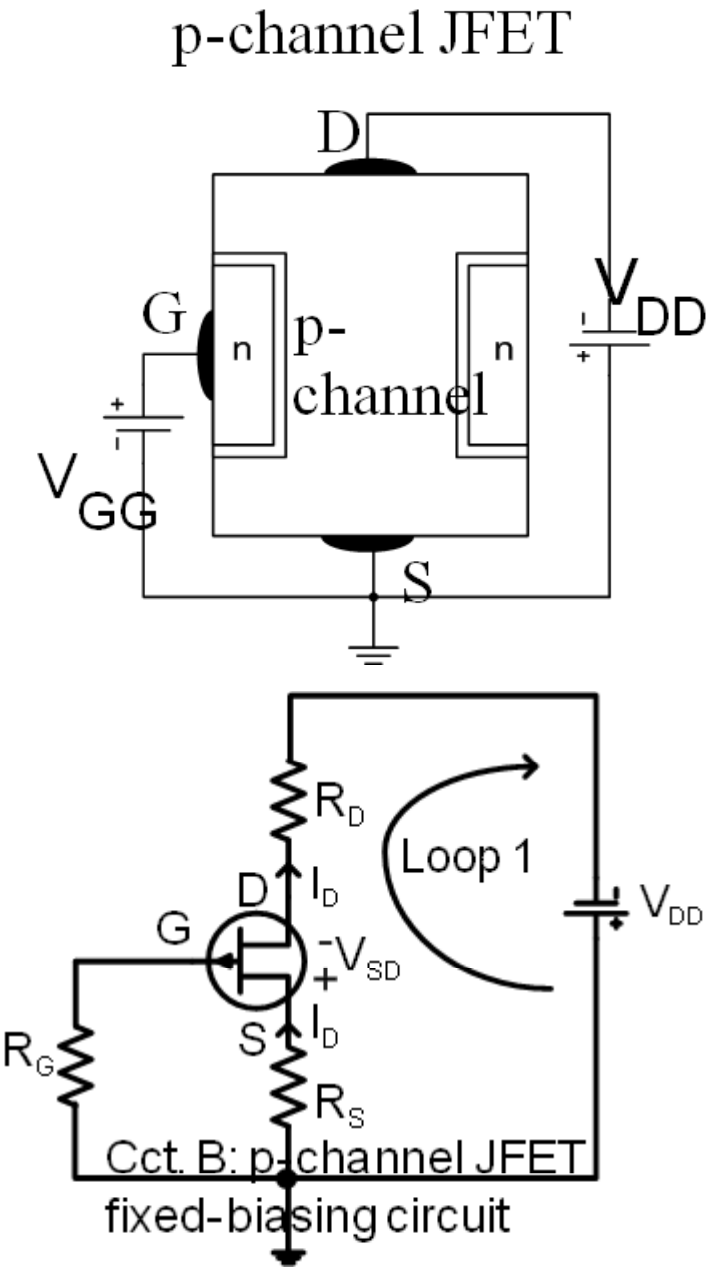
In Cct. A:

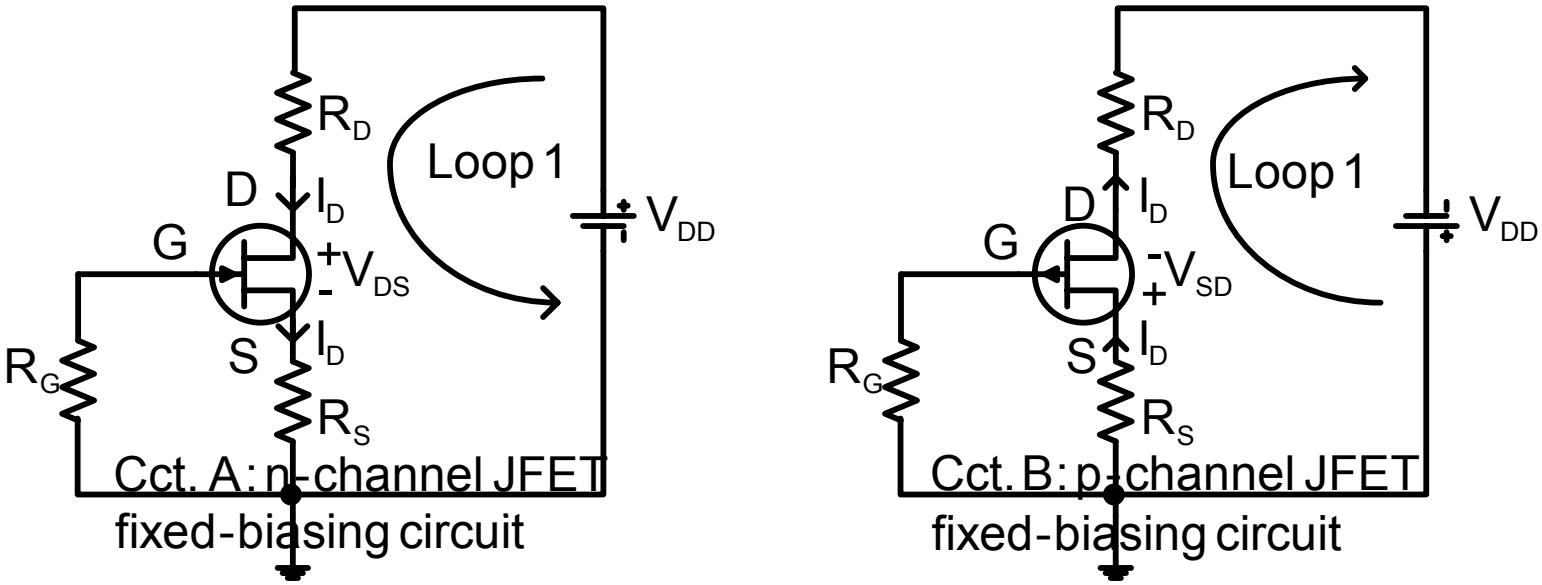
- $-V_{DD} + I_D R_D + V_{DS} + I_D R_S = 0.$
- $I_D R_D + V_{DS} + I_D R_S = V_{DD}.$
- $V_S = I_D R_S$ is positive.
- Since $I_G \approx 0$, then $V_{RG} \approx 0$. Hence, $V_G = 0$.
- Since $V_G = 0$ and V_S is positive, $V_{GS} = V_G - V_S$ = negative.
- So, the n-channel is properly biased as an amplifier.
- $V_{GS} = -V_S = - I_D R_S.$
- $R_S = V_S / I_D.$



In Cct. B:

- $I_D R_S + V_{SD} + I_D R_D - V_{DD} = 0$.
- $I_D R_S + V_{SD} + I_D R_D = V_{DD}$.
- $V_S = - I_D R_S$.
- V_S is negative.
- Since $I_G \approx 0$, then $V_{RG} \approx 0$. Hence, $V_G = 0$.
- Since $V_G = 0$ and V_S is negative, $V_{GS} = V_G - V_S$ = positive.
- So, the p-channel is properly biased as an amplifier.
- $V_{GS} = -V_S = I_D R_S$.
- $R_S = V_{GS} / I_D$.
- For both n- and p-channel JFET, $R_S = |V_{GS}| / I_D$.





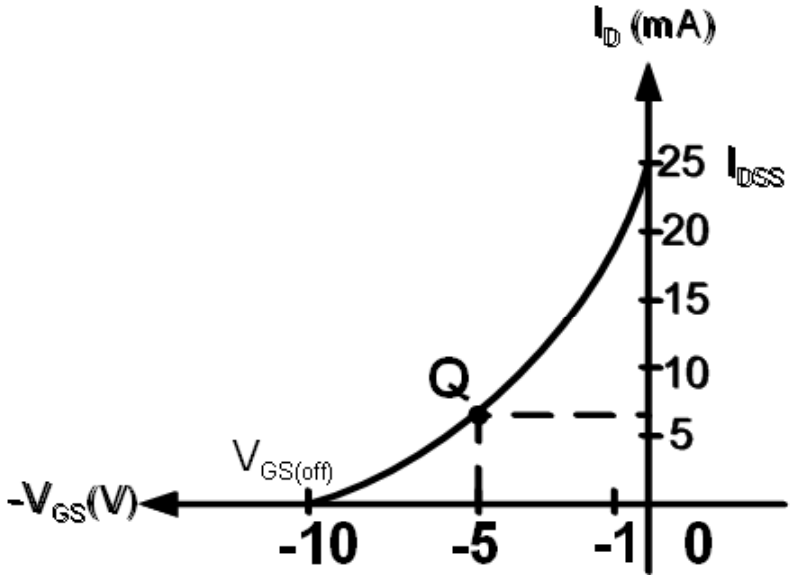
- **In the JFET, majority carriers are moving from S to D.**
- **In the n-channel JFET, V_{DD} is positive to attract the electrons to move from S to D. Conventional current flow is opposite to the flow of electron. Hence, the direction of current is from D to S.**
- **In the p-channel JFET, V_{DD} is negative to attract the holes to move from S to D. Conventional current flow is the same as the flow of holes. Hence, the direction of current is from S to D.**

Determining the operational point of the self-biasing JFET

2 ways:

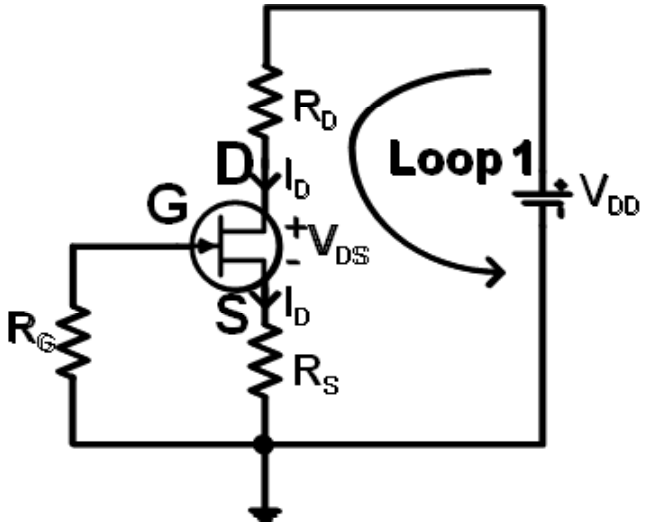
1. **graphical method, i.e. from the transfer and drain characteristic**
2. **from calculation, i.e. using:**

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$



Example 1

Determine the R_S that is needed to self bias an n-channel JFET that has the transfer characteristic curve as shown at V_{GS} = -5 V.



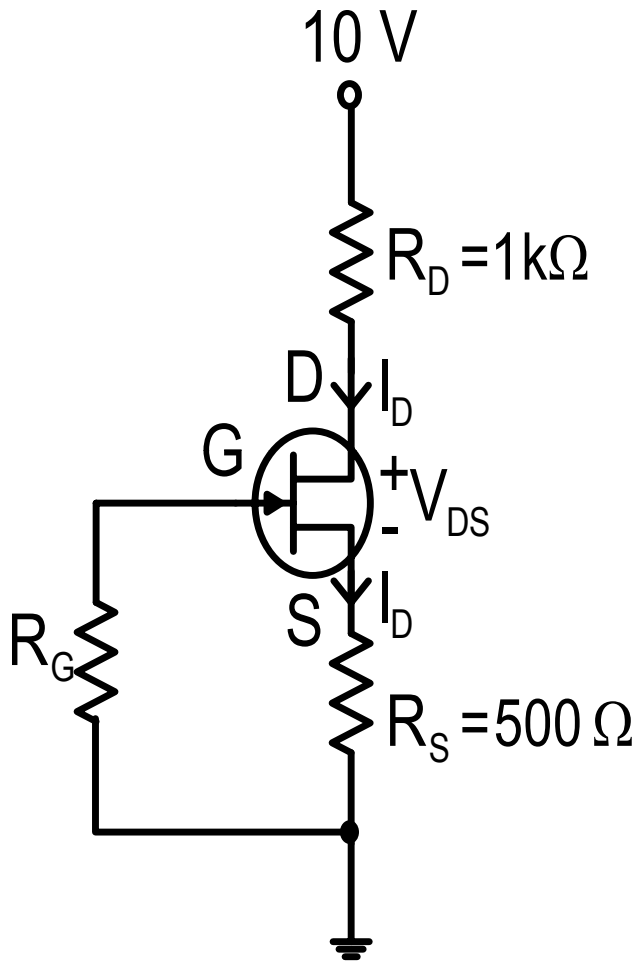
Solution

From the graph, at V_{GS} = -5 V, I_D=6.25mA.

$R_S = |V_{GS}| / I_D = 5 / 6.25\ m = 800\ \Omega$

Example 2

Determine V_{DS} and V_{GS}. Given I_D = 5 mA.



Solution:

V_G = 0 V (criteria of the self-biased circuit).

V_S = $I_D R_S$ = 5m x 500 = 2.5 V

V_{GS} = - V_S

V_{GS} = -2.5 V

V_{DD} = $I_D R_D$ + V_{DS} + $I_D R_S$

V_{RD} = $I_D R_D$ = 5m x 1k = 5 V

V_{RS} = $I_D R_S$ = V_S = 2.5 V

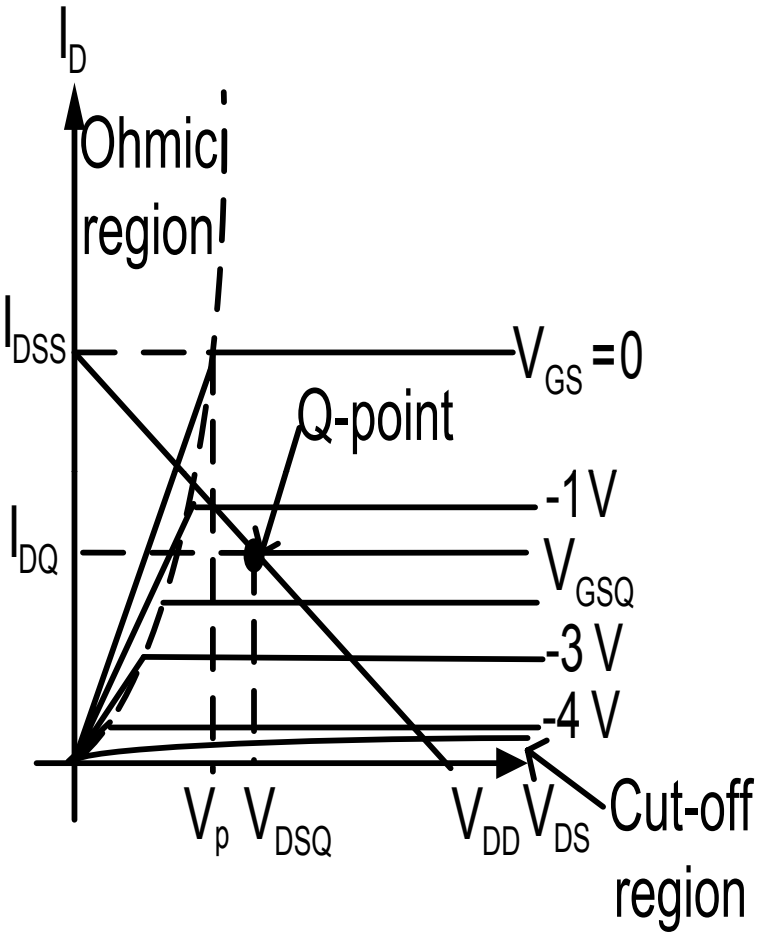
V_{DS} = 10 – 5 – 2.5 = 2.5 V

3. **Mid-point biasing**

The JFET is typically biased near the mid-point of the drain characteristic curve to achieve maximum signal swing at the input. The purpose is to obtain maximum undistorted ouput signal.

Steps to obtain the Q-point

1. **Mid-point biasing enables maximum drain current swing between I_{DSS} and 0. $I_{DQ} = I_{DSS}/2$.**
2. **From** $$I_D = I_{DSS}\left[1 - \frac{V_{GSQ}}{V_{GS(off)}}\right]^2$$ **and when $I_{DQ}=I_{DSS}/2$, $V_{GSQ}=V_{GS(off)}/3.4$**
3. **To set the drain voltage at mid-point, $V_{DQ} = V_{DD}/2$**



4. **Choose large R_G to prevent loading effect. R_G = 1 MΩ**

Example 3

Determine the resistors to be implemented in the following circuit for mid-point biasing. The parameters for the JFET are: I_{DSS} = 15 mA and $V_{GS(off)}$ = -8 V.

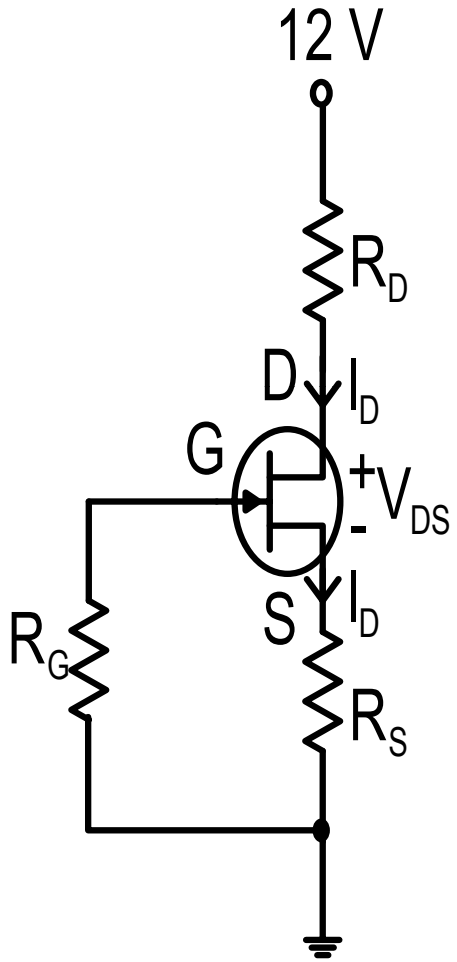
Solution

$$I_{DQ} = \frac{I_{DSS}}{2} = 7.5 \text{ mA}$$

$$V_{GSQ} = \frac{V_{GS(off)}}{3.4} = \frac{-8}{3.4} = -2.35 \text{ V}$$

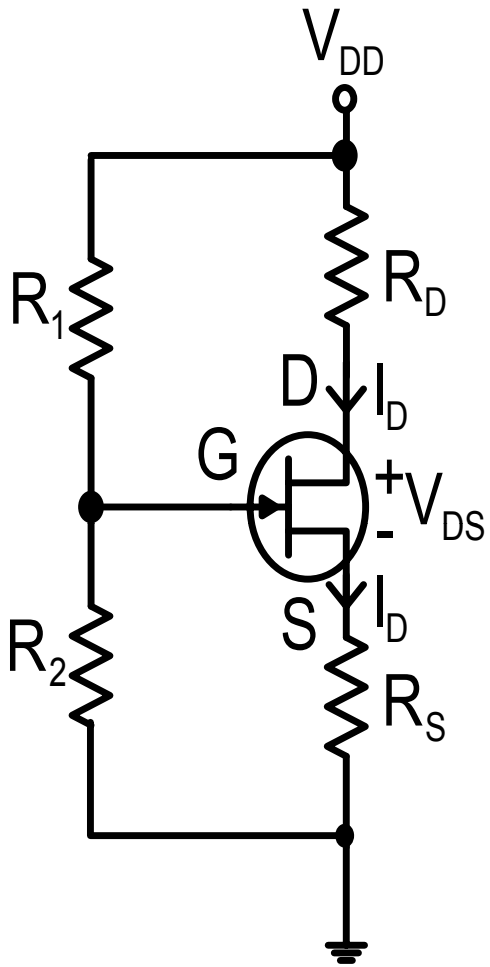
$$V_{DQ} = \frac{V_{DD}}{2} = \frac{12}{2} = 6 \text{ V}$$

- R_G = 1 MΩ
- $V_{GSQ} = - V_S$
- $V_{SQ} = 2.35 \text{ V} = I_{DQ}R_S$
- $R_S = V_{SQ} / I_{DQ} = 2.35 / 7.5 \text{ m} = 313 \Omega$
- $R_D = V_{DD} - V_{DQ} / I_{DQ} = (12 - 6) / 7.5 \text{ m} = 800 \Omega$



Voltage-divider bias.

- **V_S has to be more positive than V_G to maintain the requirement of a reverse biased G-S.**
- **$V_S = I_D R_S$**
- $$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD}$$



Example 4

Determine I_D and V_{GS} for the following voltage-divider biased JFET. Given V_{DD} = 12 V, V_D = 7 V, R_D = 3.3 kΩ, R_S = 1.8 kΩ, R_1 = 6.8 MΩ and R_2 = 1 MΩ.

Solution:

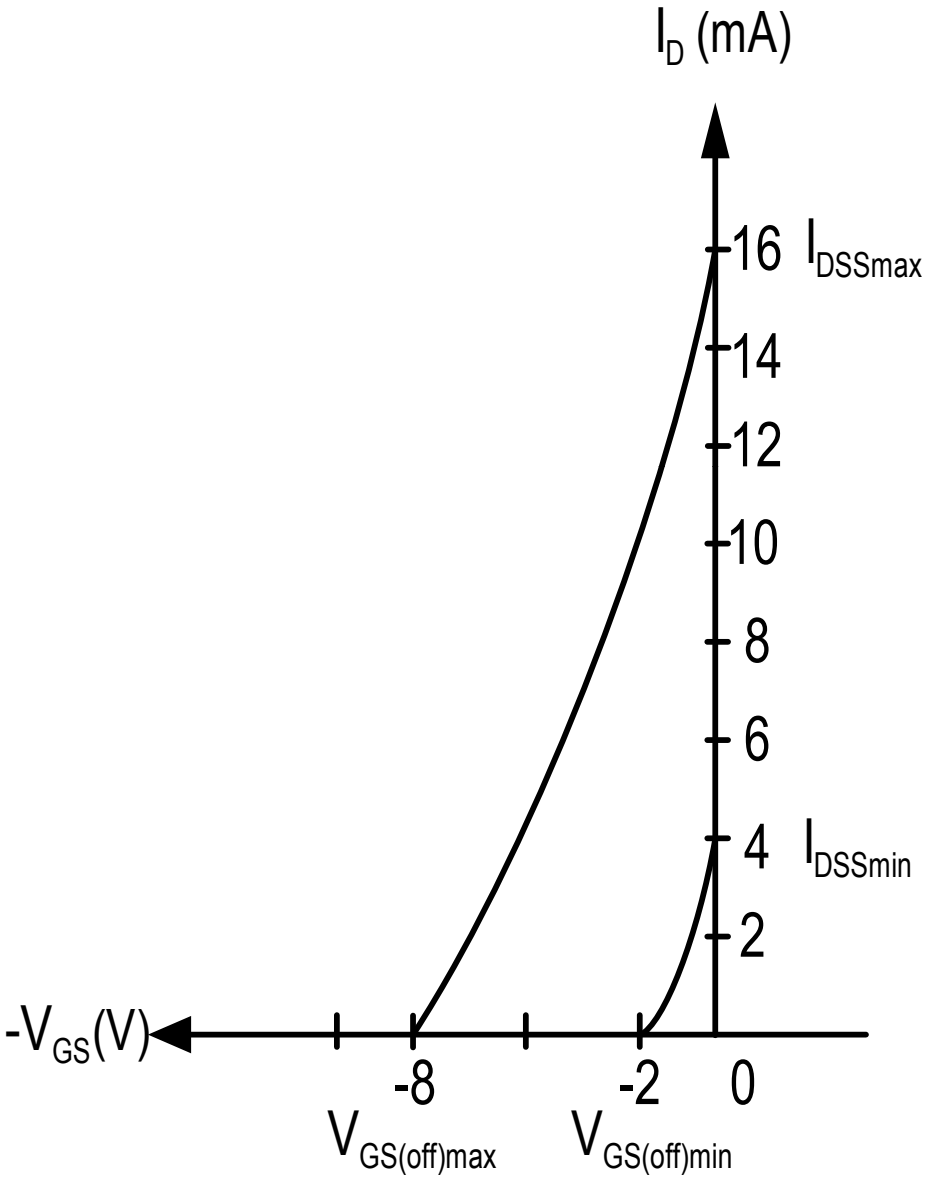
$$I_D = \left(\frac{V_{DD} - V_D}{R_D} \right) = \left(\frac{12 - 7}{3.3\ k} \right) = 1.52\ mA$$

$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{1M}{6.8\ M + 1M} \right) 12 = 1.54\ V$$

- **$V_S = I_D R_S$ = 1.52 m x 1.8 k = 2.74 V**
- **$V_{GS} = V_G - V_S$ = 1.54 – 2.74 = -1.2 V**

Q-point stability

Looking at the data sheet for 2N5459, the $V_{GS(off)}$ is in the range of -2 V to -8 V and I_{DSS} is from 4 mA to 16 mA. So, the transfer characteristic of the JFET can differ considerably from one device to the other although they are from the same type. If a 2N5459 in a bias circuit is replaced with another 2N5459, the transfer characteristic curve can vary greatly as shown in the diagram. If a 2N5459 is randomly chosen, the operating point can be anywhere within these 2 curves.



For the shown circuit, $V_{GS} = -I_D R_S$. The JFET is 2N5459. To determine the Q-point of the circuit, a dc load line is established. The load line can be established by determining 2 points:

1. **the V_{GS} when $I_D = 0$**
2. **the V_{GS} when $I_D = I_{DSS}$**

$V_{GS} = -I_D R_S$.

When $I_D = 0$, $V_{GS} = 0$.

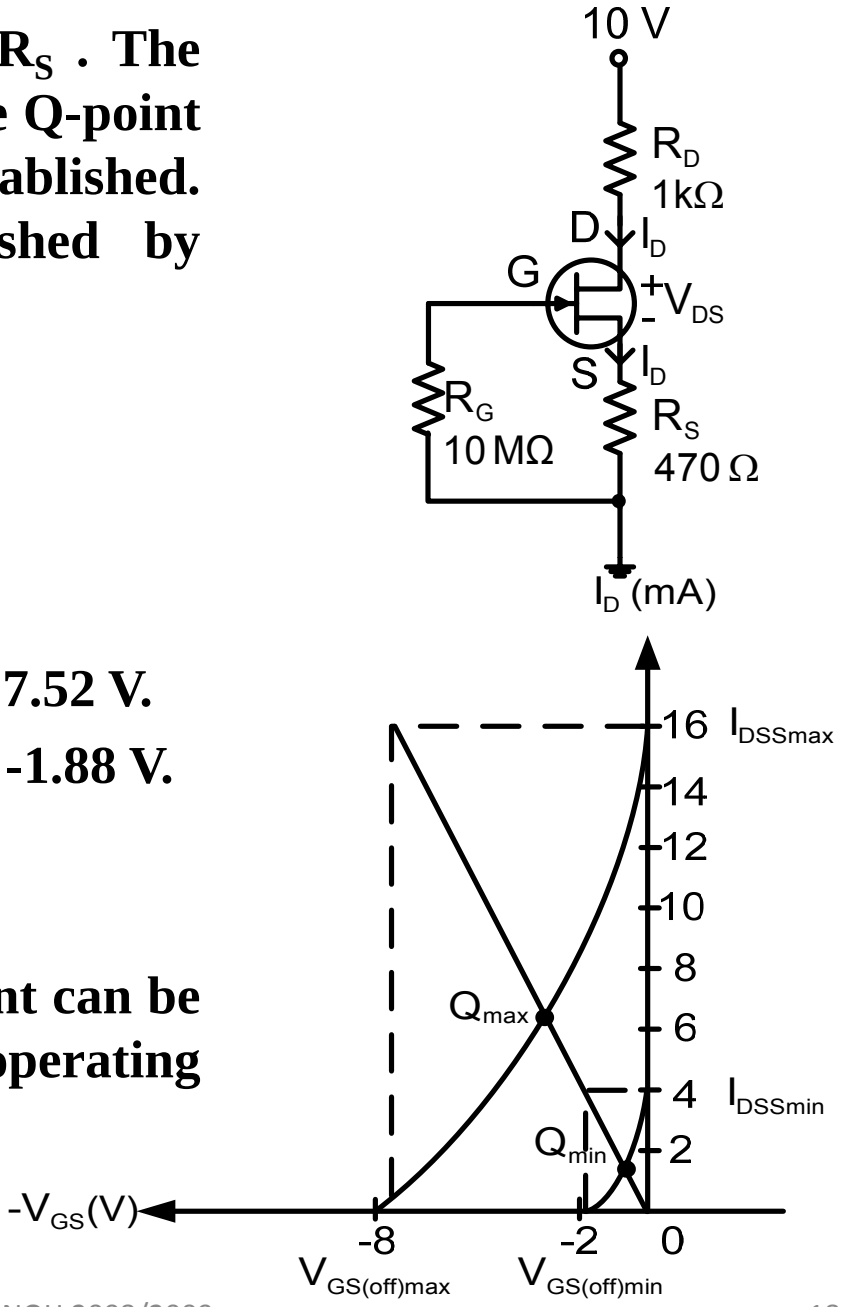
When $I_D = I_{DSSmax}$, $V_{GS} = -16m(470) = -7.52$ V.

When $I_D = I_{DSSmin}$, $V_{GS} = -4\ m(470) = -1.88$ V.

Q_{max}: $I_{DQ} = 6.25$ mA, $V_{GSQ} = -3$ V.

Q_{min}: $I_{DQ} = 1.5$ mA, $V_{GSQ} = -0.8$ V.

It is seen that the operating current can be as different as 4.75 mA and the operating voltage can vary as much as 2.2 V.



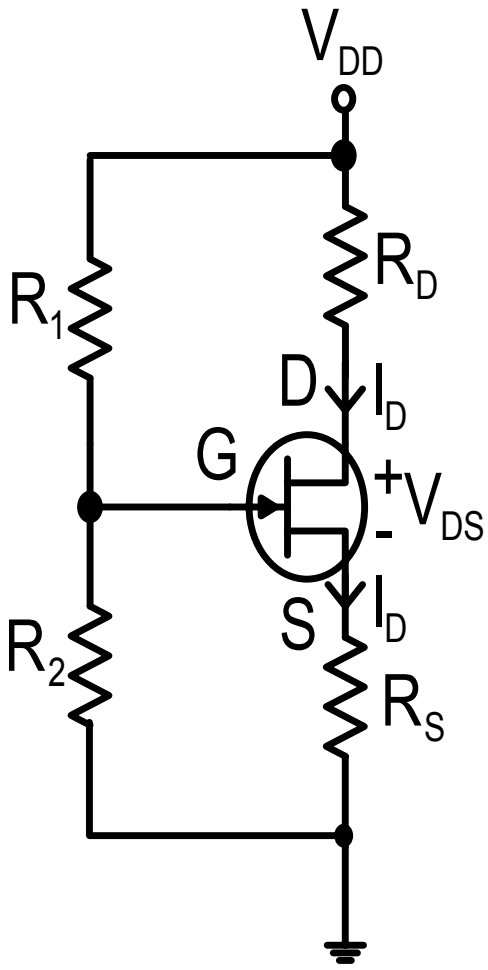
For the voltage-divider bias circuit,

- $V_S = I_D R_S$
- $V_G = (R_2 V_{DD}) / (R_1 + R_2)$
- $V_{GS} = V_G - V_S$

  To draw the load line on the transfer characteristic:

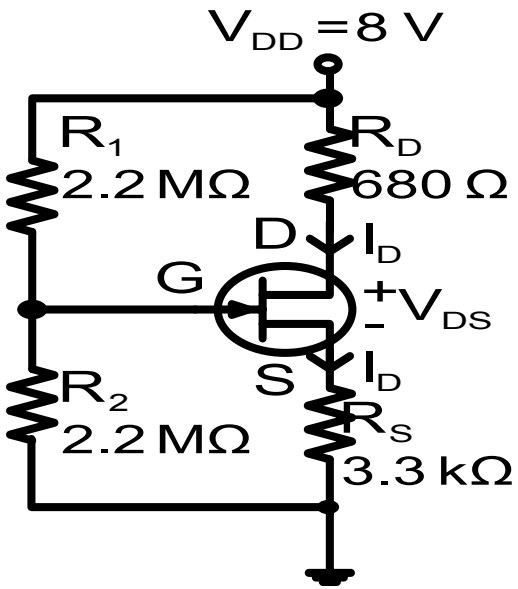
1. **determine V_{GS} when $I_D = 0$,**
2. **determine I_D when $V_{GS} = 0$.**

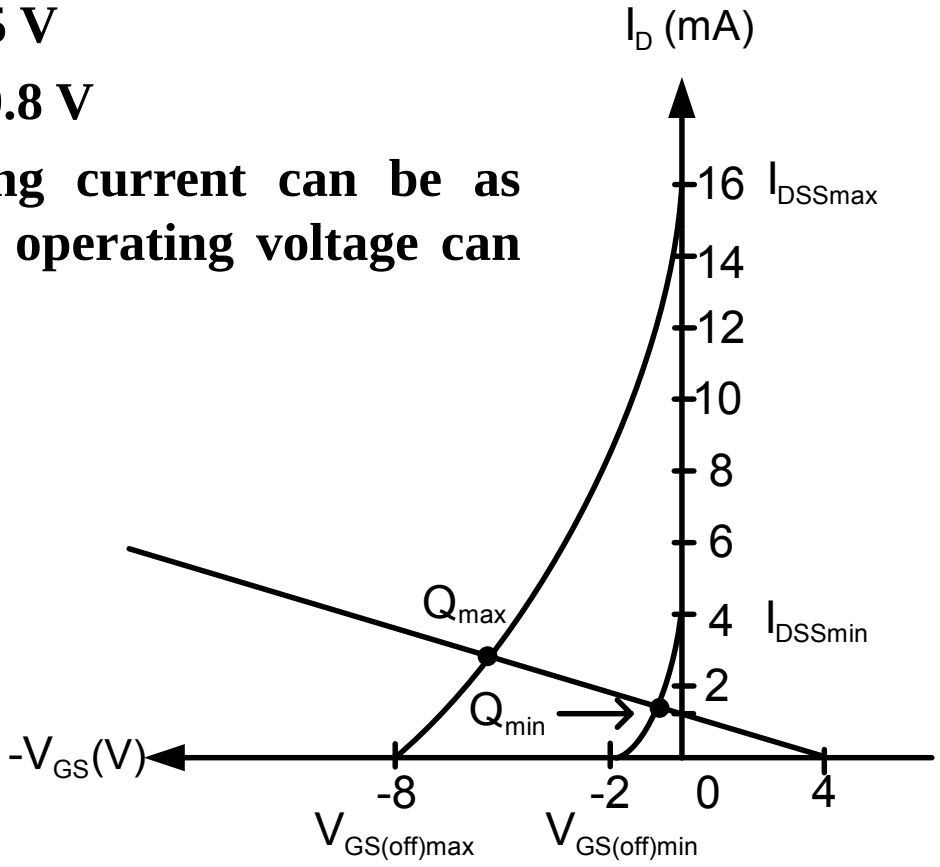
- **If $I_D = 0$, $V_S = 0$ and $V_{GS} = V_G$.**
- **If $V_{GS} = 0$, $V_S = V_G = I_D R_S$.**
- **Hence, $I_D = V_G / R_S$.**



Example:

- $V_G = (R_2 V_{DD}) / (R_1 + R_2) = (2.2\ M \times 8) / 4.4\ M = 4\ V.$
- For $I_D = 0$, $V_S = 0$ and $V_{GS} = V_G = 4\ V.$
- If $V_{GS} = 0$, $I_D = V_G / R_S = 4 / 3.3\ k = 1.2\ mA.$
- Q_{max}: $I_{DQ} = 3\ mA$, $V_{GSQ} = -4.5\ V$
- Q_{min}: $I_{DQ} = 1.5\ mA$, $V_{GSQ} = -0.8\ V$
- It is seen that the operating current can be as different as 1.5 mA and the operating voltage can vary as much as 3.7 V.





Bias cct. type	ΔI_{DQ} (mA)	ΔV_{GSQ} (V)
Self-bias	4.75	2.2
Voltage-divider	1.5	3.7

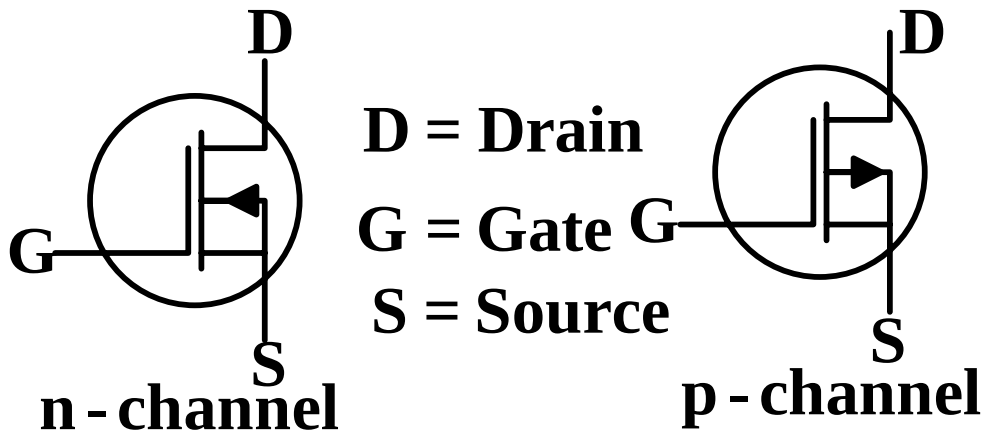
I_D is much more stable with voltage-divider bias. This is because the slope of the load line is less than for the self-bias. The variation of the G-S voltage for the voltage-divider circuit is slightly more than the one for the self-bias circuit.

METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

The MOSFET is the second category of the FETs. The MOSFET differs from the JFET in that it has no p-n junction; instead, the G of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. The two basic types of MOSFETs are the depletion (D-MOSFET) and the enhancement (E-MOSFET). Because of the insulated G, these devices are also known as the IGFETs.

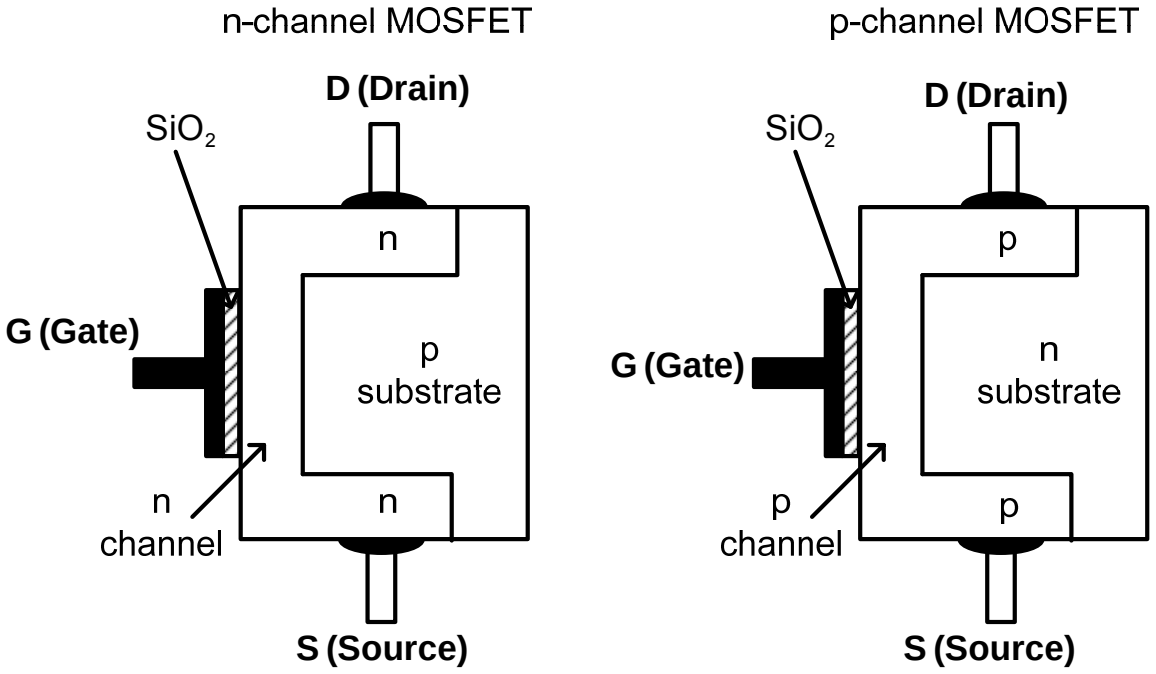
Symbol for the n channel and p channel D-MOSFET

The substrate, indicated by the arrow, is normally (but not always) connected internally to the S. Sometimes, there is a separate substrate pin.



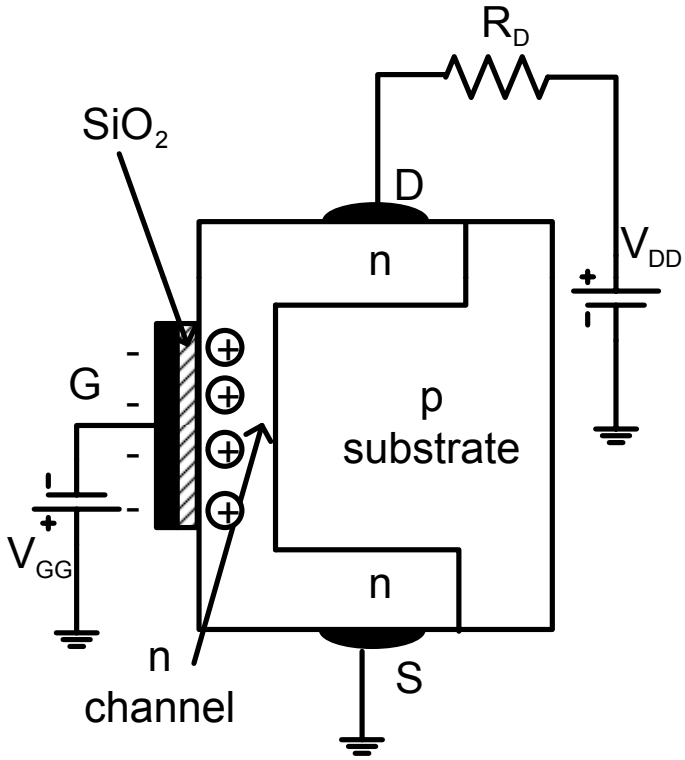
Depletion MOSFET (D-MOSFET)

- **The D and S are connected by a narrow channel adjacent to the insulated G. The D-MOSFET can be operated in either of two modes – the depletion mode or the enhancement mode. Thus, the D-MOSFET is also known as the depletion/enhancement (DE-) MOSFET.**
- **G-SiO_2-channel form a parallel plate capacitor (G and channel are the two parallel plates, SiO_2 insulating layer is the dielectric).**



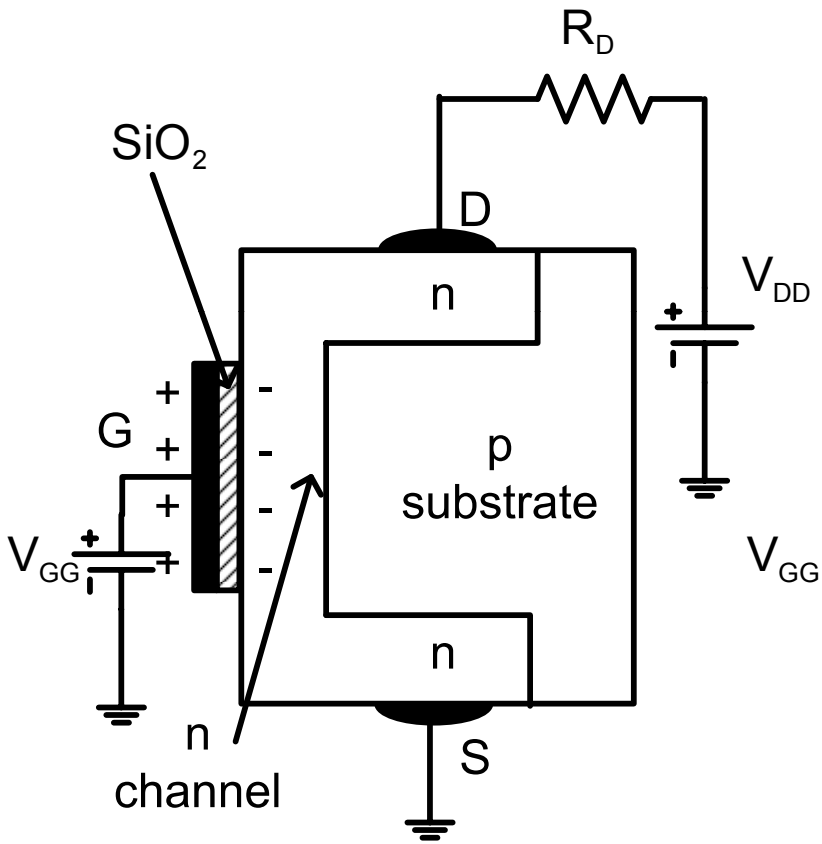
Depletion mode (negative V_{GS}) n channel D-MOSFET

Negative charges on the G repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the n channel is depleted of some of its electrons, thus decreasing the channel's conductivity. The greater the negative voltage on the G, the greater the depletion of n channel electrons. At a sufficiently negative G-S voltage ($V_{GS(off)}$), the channel is totally depleted and the drain current (I_D) is zero.

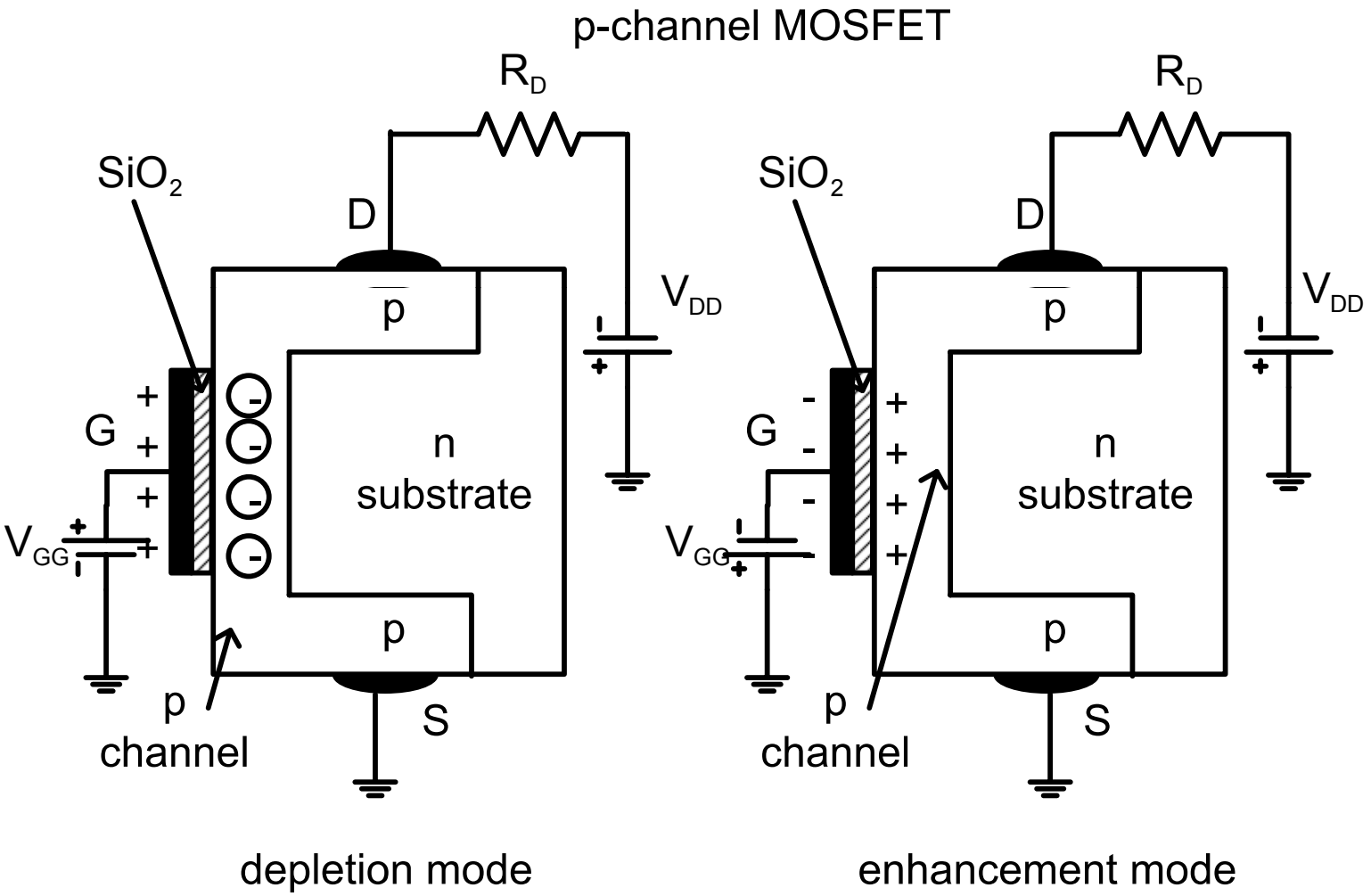


Enhancement mode (positive V_{GS}) n channel D-MOSFET

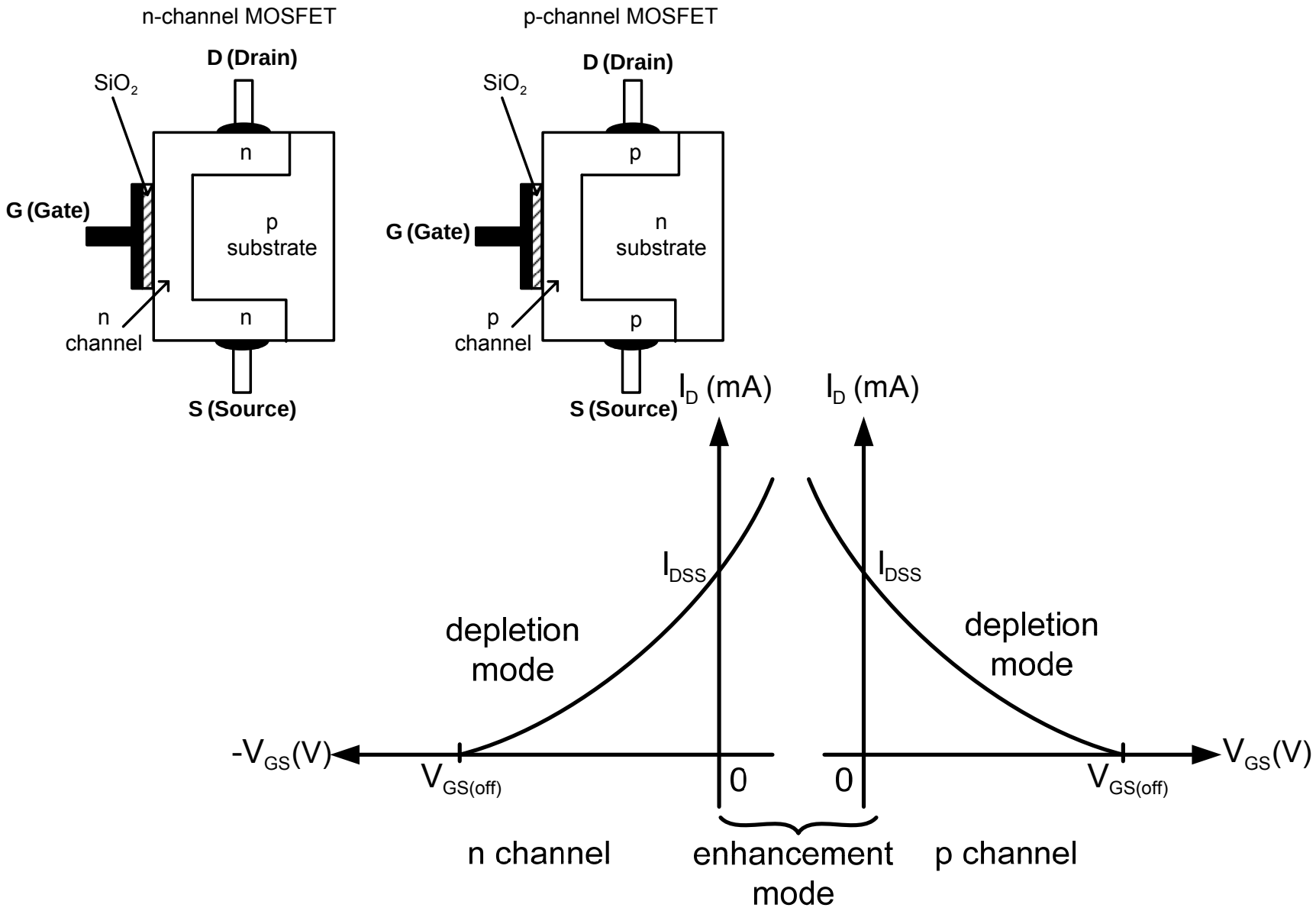
With a positive G voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel's conductivity. The greater the positive voltage on the G, the greater the conductivity of the n channel, thus increasing the drain current, I_D.



Enhancement (negative V_{GS}) and depletion (positive V_{GS}) modes of the p channel D-MOSFET



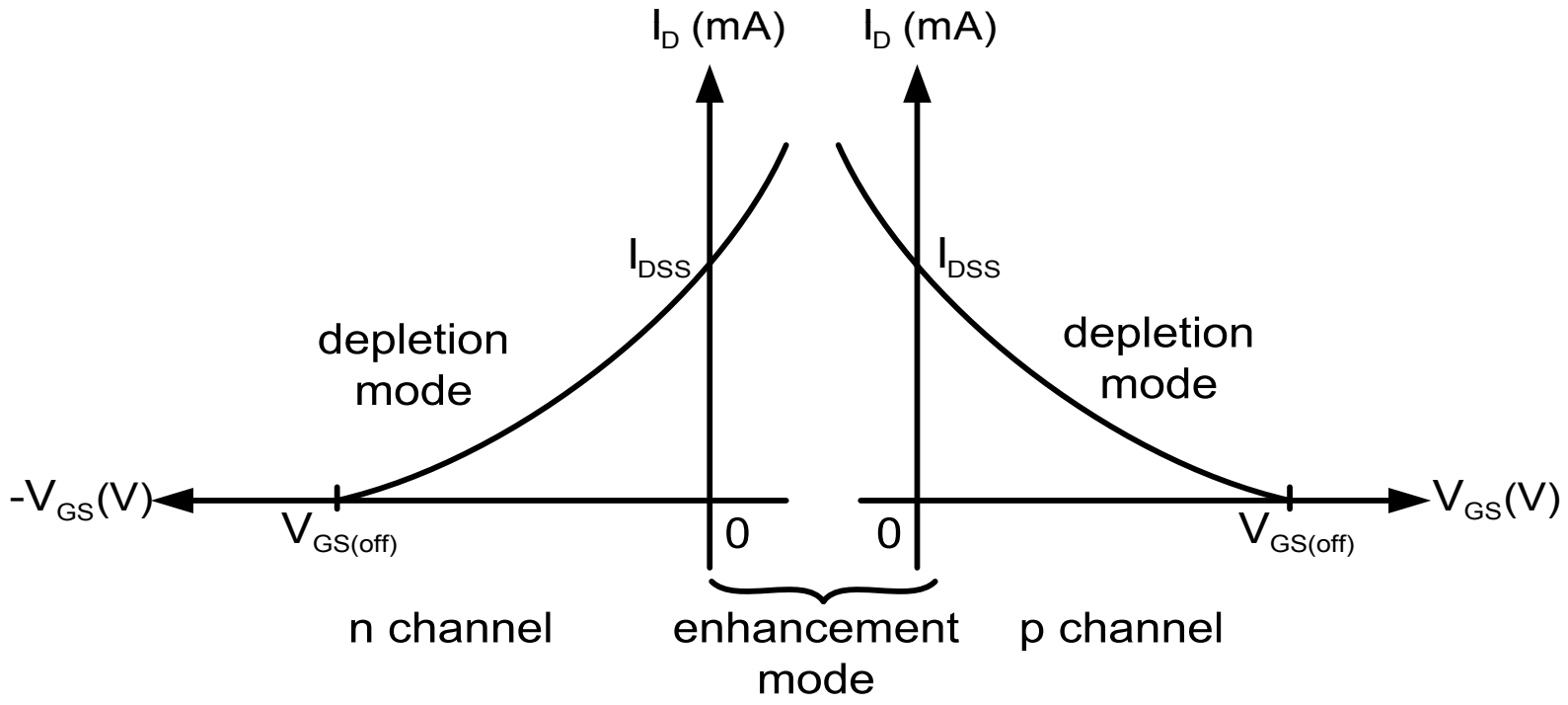
D-MOSFET transfer characteristic



D-MOSFET can operate with either positive or negative gate voltages. The point on the curves where $V_{GS} = 0$ corresponds to I_{DSS}. The point where $I_D = 0$ corresponds to $V_{GS(off)}$. As with the JFET, $V_{GS(off)} = -V_p$. The square-law expression for the JFET curve,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

also applies to the D-MOSFET curve.



Example

For a certain D-MOSFET, I_{DSS} = 10 mA and $V_{GS(off)}$ = -8 V.

(a) Is this an n-channel or a p-channel?

(b) Calculate I_D at V_{GS} = -3 V.

(c) Calculate I_D at V_{GS} = 3 V.

Solution

(a) This is an n-channel D-MOSFET as the $V_{GS(off)}$ is negative.

(b) $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 = 10\ m\left[1 - \frac{(-3)}{(-8)}\right]^2 = 3.91\ mA$$

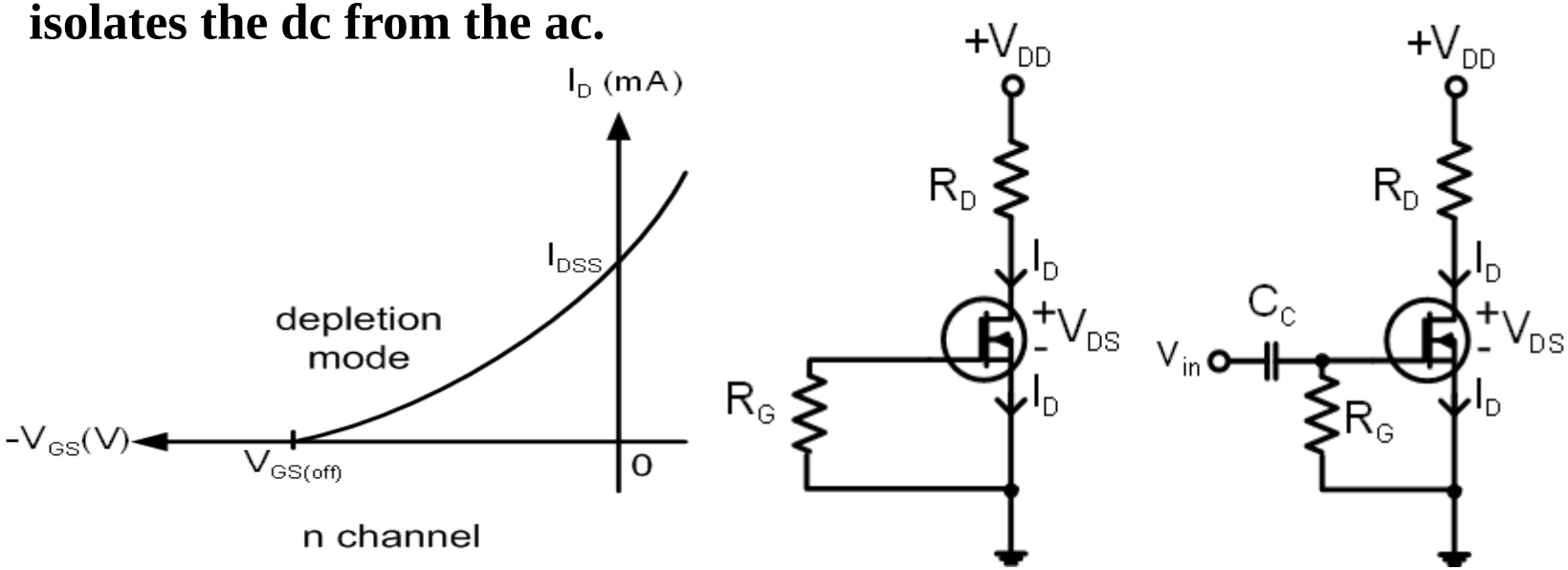
(c) $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 = 10\ m\left[1 - \frac{(3)}{(-8)}\right]^2 = 18.91\ mA$$

From the answers for (b) and (c), it is observed that if V_{GS} is negative, $I_D < I_{DSS}$. This is the operation of the n-channel D-MOSFET in the depletion mode. If the V_{GS} is positive, $I_D > I_{DSS}$ and this indicates that the transistor is operating in its enhancement mode.

D-MOSFET Bias – Zero bias

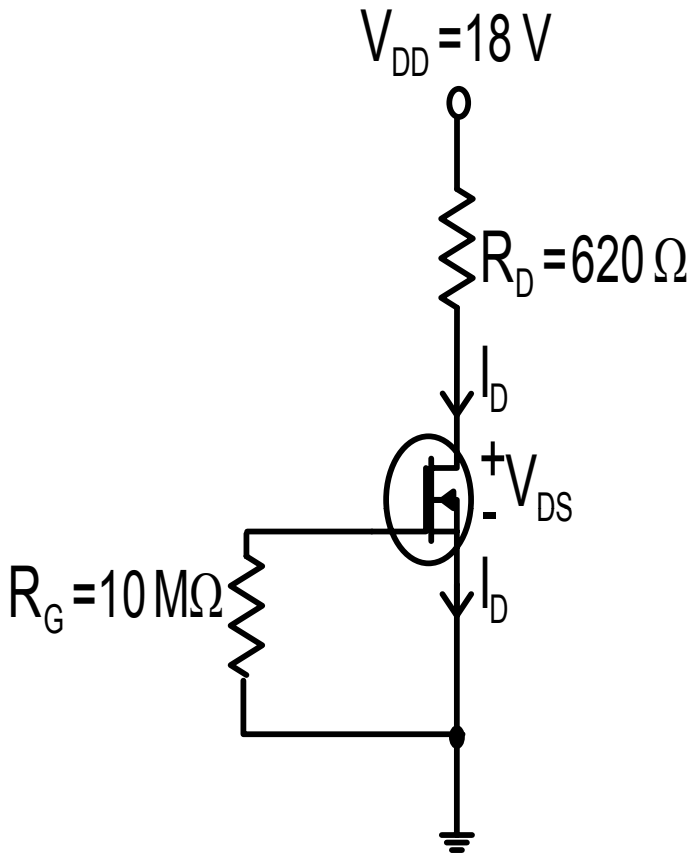
As the D-MOSFET can be operated with either positive or negative values of V_{GS}, a simple bias method is to set $V_{GS} = 0$ so that an ac signal at the G varies the G-S voltage above and below this 0 V bias point.

- **$V_S = 0$ and $V_G = 0$ as $I_G = 0$. Hence, $V_{GS} = 0$. For $V_{GS} = 0$, $I_D = I_{DSS}$.**
- **$V_{DS} = V_{DD} - I_D R_D = V_{DD} - I_{DSS} R_D$**
- **The purpose of the R_G is to accommodate an ac signal input by isolating it from ground. Since there is no dc gate current, R_G does not affect the zero G-S bias. C_C is the coupling capacitor which isolates the dc from the ac.**



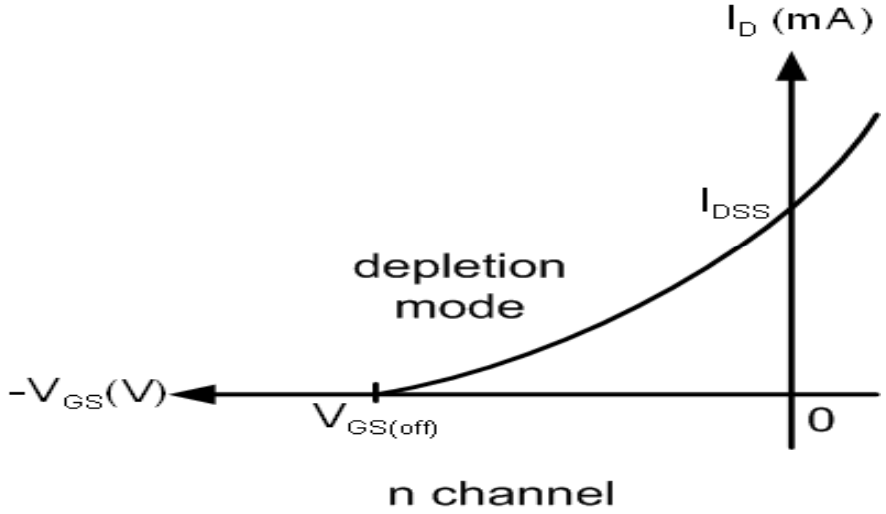
Example

Determine V_{DS} for the shown circuit. The MOSFET data sheet gives $V_{GS(off)}$ = -8 V and I_{DSS} = 12 mA.



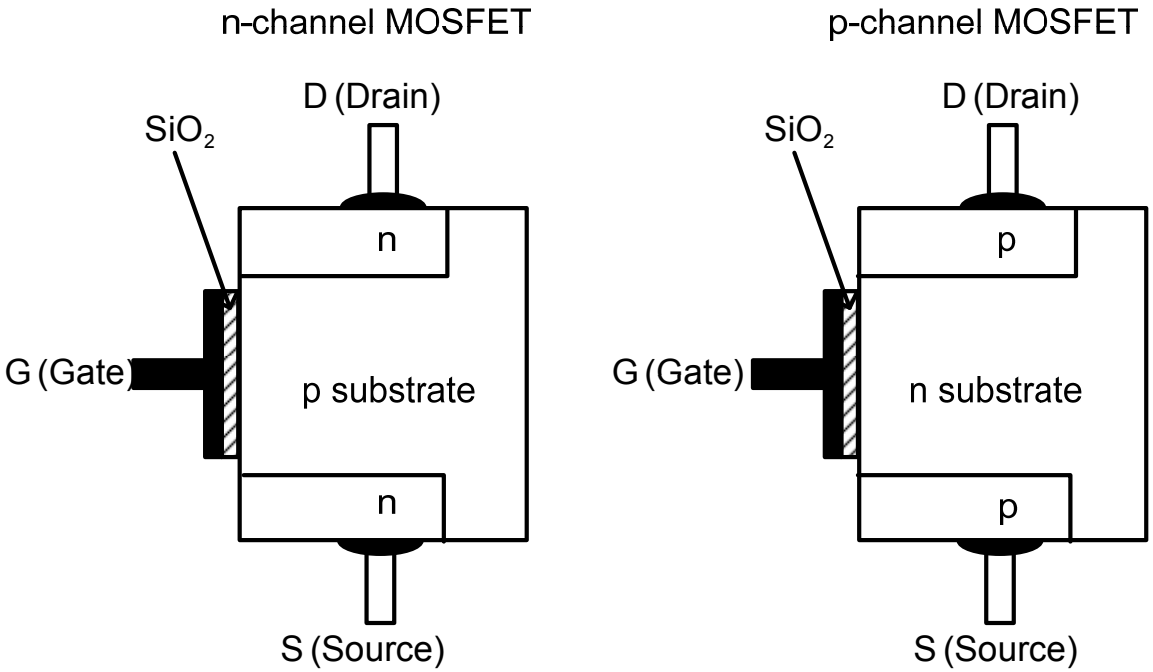
Solution

- $I_D = I_{DSS} = 12$ mA.
- $V_{DS}=V_{DD}-I_{DSS}R_D=18–12m(620)=10.56V.$

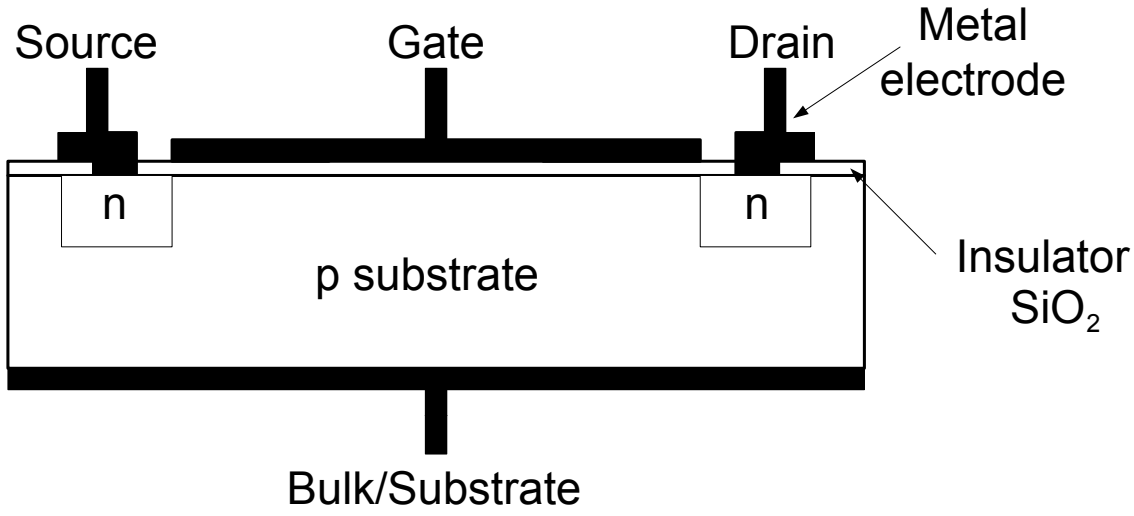


Enhancement MOSFET (E-MOSFET)

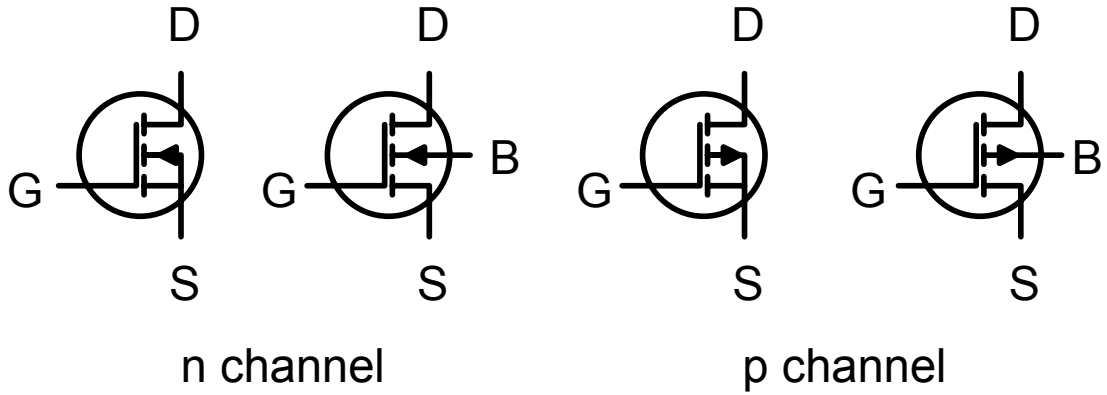
- **The E-MOSFET only operates in the enhancement mode and has no depletion mode. It differs in construction from the D-MOSFET in that it does not have a structural/physical channel.**
- **In an E-MOSFET, the substrate extends completely to the SiO_2 layer. Notice that there is no physical channel between S and D, like the one available in D-MOSFET.**



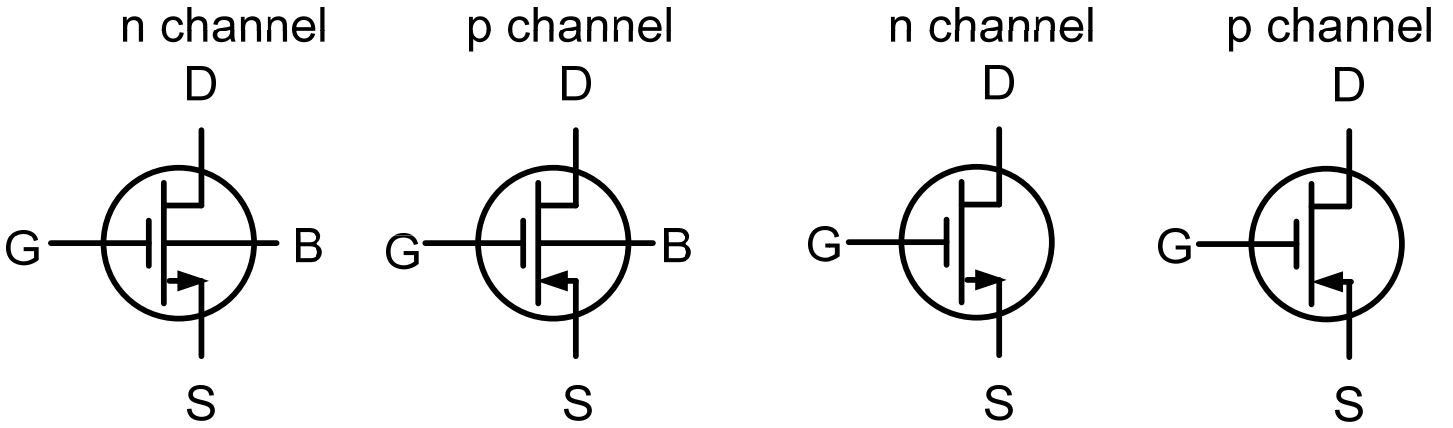
Cross section of conventional E-MOSFET structure is shown below:



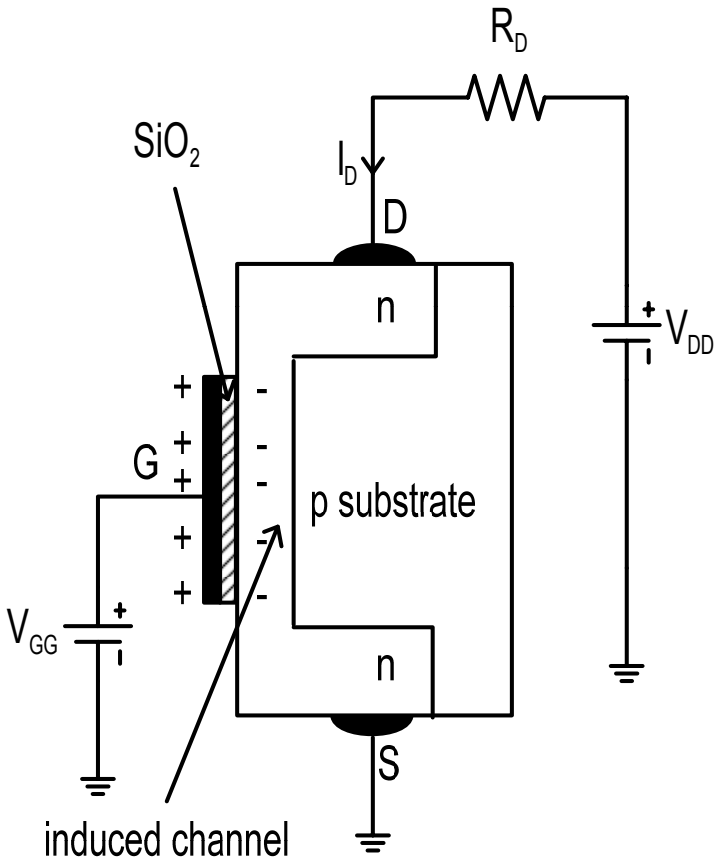
Schematic symbols for the E-MOSFET are shown below. The broken lines symbolize the absence of a physical channel.



The symbols of the E-MOSFET in the circuit schematics are also normally obtained in the following forms:

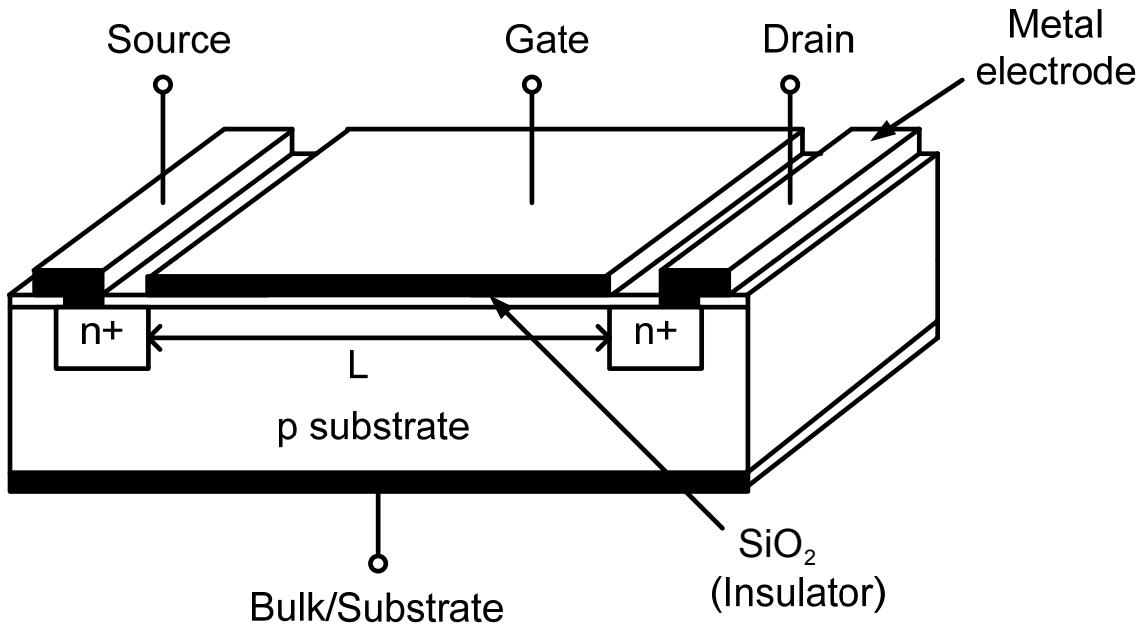


For the n-channel E-MOSFET, a positive gate above a threshold voltage induces a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer. The conductivity of the channel is enhanced by increasing the V_{GS} which can attract more electrons into the channel area. For any G voltage below the threshold value, there is no channel.



E-MOSFET Operation

Cross-section diagram of an E-MOSFET:

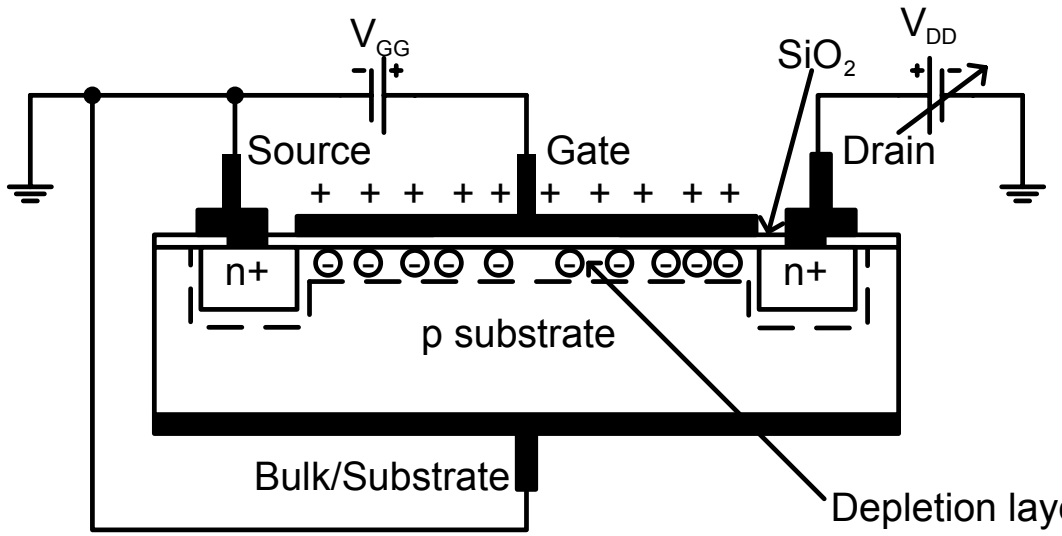


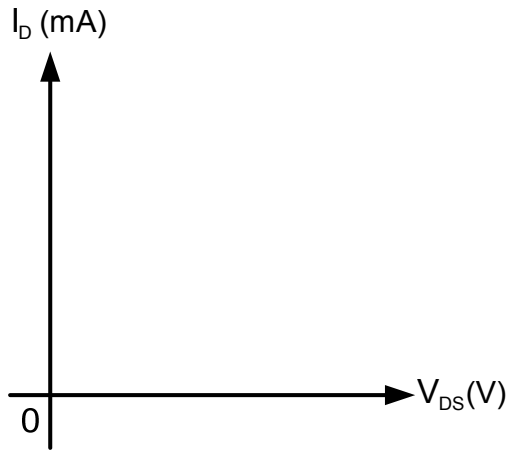
1. **<u>When V_{DS} = 0 and V_{GS} = 0</u>**

   If V_{GS} = 0, there will be no channel induced. Besides this, V_{DS} = 0 and therefore no electrons are flowing from S to D. Hence, I_D = 0.

2. When $V_{GS} < V_{GS(th)}$

The p substrate underneath the G forms a depletion layer as holes move further into the bulk, away from this area. Fixed negative ions will be left in this depletion layer. As S and D are separated by the depletion layer and the lowly doped p, no current will flow even though V_{DS} is available and positive. In this circuit, $V_{GG} = V_{GS}$ and $V_{DD} = V_{DS}$.

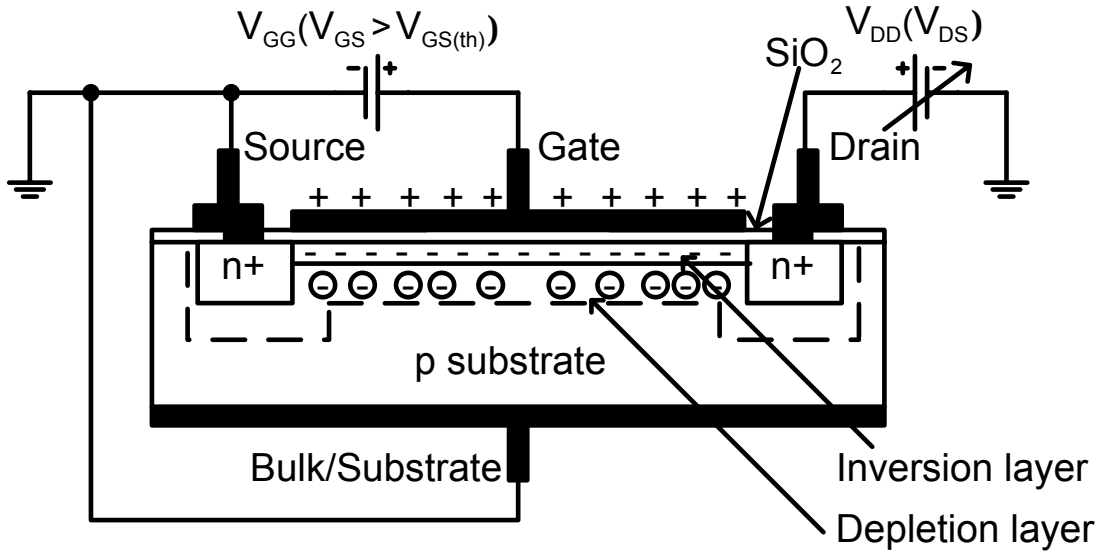




3. <u>When $V_{GS} > V_{GS(th)}$</u>

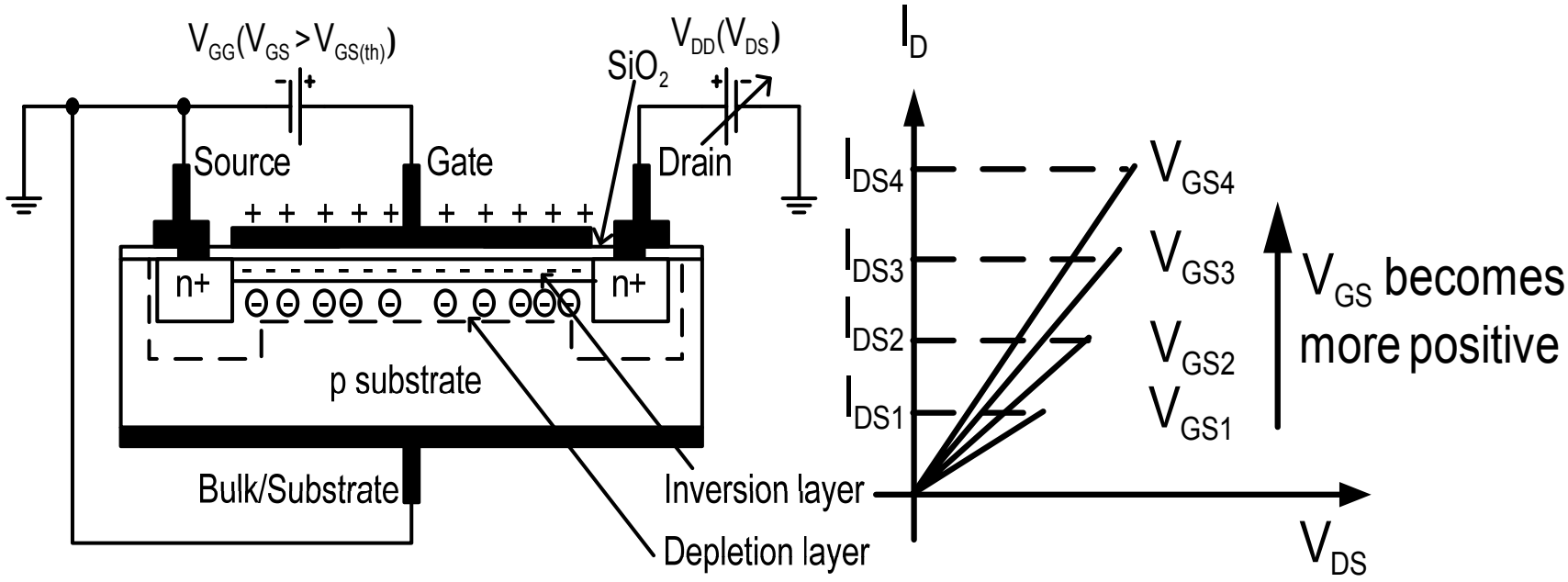
The electrons, which are the minority carriers from the substrate, and the electrons from S and D will be attracted to the region beneath the G and SiO_2. These electrons will form one layer and since they are having charges opposite to the holes of the substrate, this layer is known as the inversion layer. The inversion layer forms the channel that connects the S to D. If $V_{DS} = 0$, I_D will still be 0 as there is no movement of electrons from S to D. If $V_{DS} > 0$, electrons from S will move along the channel toward D and generate current.

- **"Enhancement" for the E-MOSFET is referring to the $V_{GS} > V_{GS(th)}$ that is required to increase or enhance the channel conductivity between D and S.**



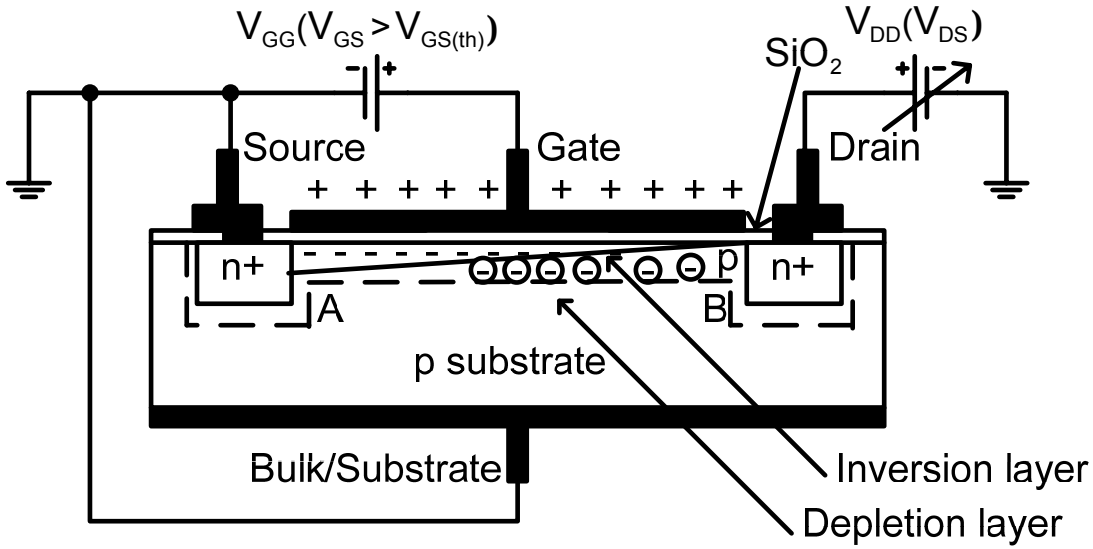
- **If V_{DS} is small, the E-MOSFET is operating as a linear resistor whose resistance is determined by the V_{GS}. When V_{GS} is large, the number of electrons in the channel is increased, conductivity of channel increases, resistance will decrease and current becomes larger.**

- **When $V_{GS} > V_{GS(th)}$ and V_{DS} is small, the device is said to be in its triode region of operation. Under this condition, $I_D \propto (V_{GS} - V_{GS(th)})V_{DS}$. So, if $V_{GS} > V_{GS(th)}$ and $V_{DS} > 0$, I_D will exists. If V_{DS} is increased, I_D will also increase as more electrons will be able to flow from S to D.**

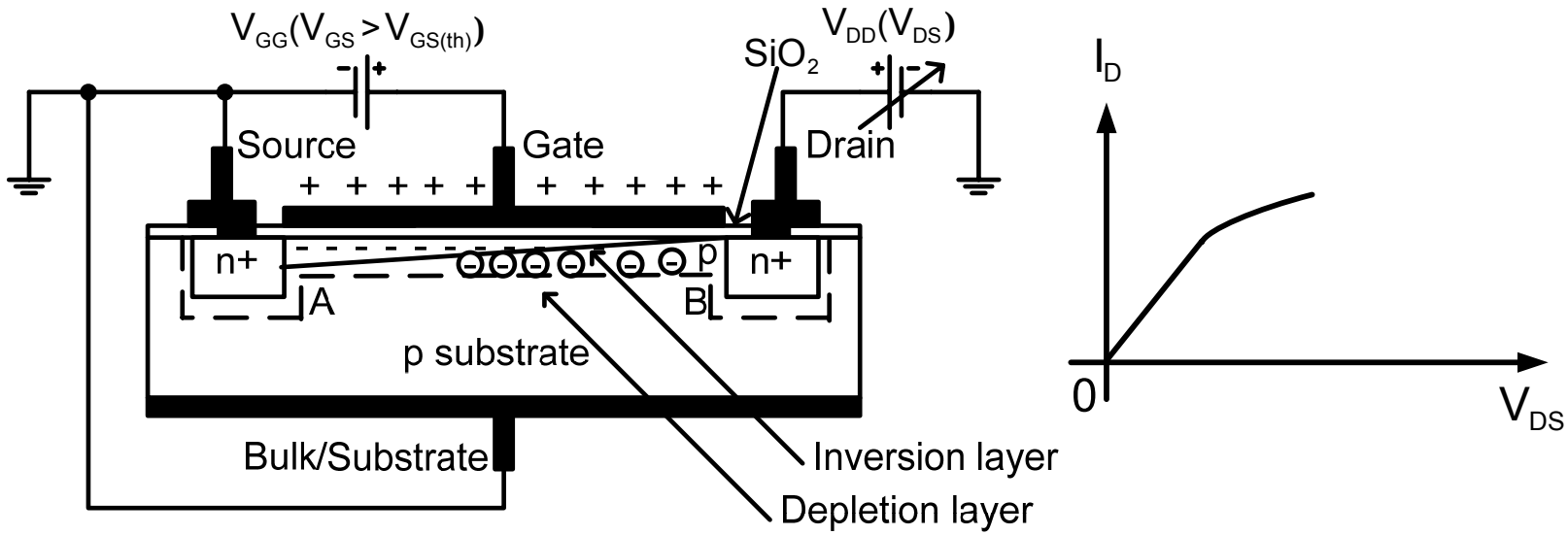


4. <u>When $V_{GS} > V_{GS(th)}$ and V_{DS} is increased (still $V_{DD} < V_{GG}$ i.e. $V_{DS} < V_{GS}$)</u>

- **Voltage varies along the channel, with 0 V at A (near S) and V_{DD} (or V_{DS}) at B (near D).**
- **The gate-to-channel voltage is V_{GS} at A and V_{GD} at B. The potential at A is dependent on V_{GS} and not on V_{DS}.**
- **$V_{GD} = V_G - V_D = V_{GG} - V_{DD}$**



- **$V_{GD} = V_G - V_D = V_{GG} - V_{DD}$**
- **If V_{GG} is fixed and V_{DD} is increased, V_{GD} will decrease. The width of the inversion layer is dependent on the voltage across G and the channel. Hence, the channel becomes narrower in approaching B. The channel is widest at A and narrowest at B. The conductivity at B becomes low. The I_D vs V_{DS} slope becomes lower. The current and voltage relationship is no longer linear.**



- **If V_{GD} approaches $V_{GS(th)}$, the inversion layer at B will disappear, leaving only the depletion layer. Channel is pinched-off at p. This condition occurs when $V_{DS} = V_{DS(sat)}$.**
- **$V_{GD} = V_G - V_D = V_{GS} - V_{DS} = V_{GS} - V_{DS(sat)} = V_{GS(th)}$**
- **At pinched-off, $V_{DS(sat)} = V_{GS} - V_{GS(th)}$**
- **The charge concentration of the inversion layer near D is 0. As slope = $\Delta I_D / \Delta V_{DS}$ and $\Delta I_D = 0$, the I_D vs V_{DS} slope at this point is also 0.**